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**A THESIS  
FOR THE DEGREE OF DOCTOR OF PHILOSOPHY**

**Development of Nanoscale Graphitic Devices and  
The Transport Characterization**

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**GRADUATE SCHOOL**

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博士學位論文

# Development of Nanoscale Graphitic Devices and The Transport Characterization

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***Dedicated to***

***My Beloved Mother (Late Smt. Sannuthai) for her perennial blessings***

***My father (Mr. P. Venugopal) for his endless support***

***And***

***My wife (Mrs. Latha) for her continuous encouragement and support***

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## 초록

본 학위논문에서는 그래파이트재료기반의 나노스케일 전자소자의 제작 및 전송특성에 대하여 연구를 수행하였으며, 집속이온빔의 3 차원 가공기술을 이용한 나노크기 그래파이트 적층구조접합의 제작, 단층의 그래파이트 (graphene)의 제작 및 전기전송특성분석, 그리고 산화물그래핀재료의 합성 및 전계효과트랜지스터의 전송특성에 대하여 조사하였다.

제 1 장에서는 탄소족으로 구성되는 그래파이트, 그래핀, 그래핀산화물의 전자특성과 구조등을 포함하는 기초물성을 위주로 토론했으며, 나노스케일에 이르는 그래파이트기반의 전자소자개발의 필요성에 대하여 설명하였다.

제 2 장에서는 물성특성분석 및 소자제작을 위하여 사용된 3 차원 집속이온빔가공법, 기계적박리기술 및 식각방법 등 3 가지 소작제작기술에 대하여 설명하였다.

제 3 장에서는 면내(in-plane)결정방향에 따라 제작된 그래파이트 평판형구조소자의 온도의존성에 대하여 보고하였다.

제 4 장과 5 장에서는 대면적의 면내그래파이트평판구조 (면내 혹은 c 축에 따라 제작된)의 제작 및 전기전송특성에 대하여 토론했고, 제작구조의 전기전송이방성에 대하여 간단히 기술하였다

제 6 장에서는 서브마이크론크기의 그래파이트적층구조의 제작 및 전기전송특성에 관한 소자제작 및 실험결과에 중점을 두고 설명하였으며, 다양한 면내크기 (동일적층높이)의 서브마이크론크기의 접합과 전기전송특성에 대하여 비교 설명하였다.

제 7 장에서는 나노스케일의 그래파이트 적층구조의 다양한 면내크기 및 적층높이에 따른 저항-온도의존성, 전류-전압특성 등을 조사하였다. 비선형전송특성의 발견과 그 원인에 대하여 자세히 설명 하였다.

제 8 장에서는 그래핀전계효과트랜지스터의 온도의존성에 대하여 연구하였으며, 소자제작을 위하여 식각기술과 기계적인 박리방법을 사용하였다.

마지막장인 제 9 장에서는 산화그래핀나노입자의 합성에 대하여 설명하였으며, 그래핀산화물 박막의 극저온에서의 전기전송특성에 대하여 조사하였다. 특성분석을 위하여, XRD, UV-Vis, FT-IR 그리고 SEM 관찰을 실시하였으며, 산화물그래핀 박막소자의 전계효과트랜지스터의 특성에 대하여 보고 하였다.

## Abstract

This dissertation describes the development of graphitic based nanoscale devices with its fabrication and transport characterization results. It covers graphite nanoscale stacked-junctions fabricated using focused ion beam (FIB) 3-D etching technique, a single layer graphite layer (graphene) preparation and its electrical transport characterization results and the synthesis and investigation of electrical transport behavior of graphene oxide based thin film devices.

The first chapter describes the basic information about the carbon family in detail in which the electronic properties and structure of graphite, graphene and graphene oxide are discussed. In addition, the necessity of developing nanoscale graphitic devices is given.

The second chapter explains the experimental techniques used in this research for fabricating nanoscale devices which includes focused ion beam 3-D fabrication procedures, mechanical exfoliation technique and photolithographic methods.

In third chapter, we have reported the results on temperature dependence of graphite planar-type structures fabricated along *ab*-plane.

In the fourth and fifth chapters, the fabrication and electrical transport characteristics of large in-plane area graphite planar-type structures (fabricated along *ab*-plane and *c*-axis) were discussed and their transport anisotropy properties were investigated briefly.

In the sixth chapter, we focused the fabrication of the submicron sized graphite stacked junctions and their electrical transport characterization studies. In which, FIB was used to fabricate the submicron junctions with various in-plane area (with same stack height) and their transport characteristics were compared.

The seventh chapter reports investigation of electrical transport results of nanoscale graphite stacked-junctions in which the temperature dependent transport (R-T) studies, current-voltage measurements for the various in-plane areas and for various stack height samples were analyzed. The observation of nonlinear transport characteristics and their origin were explained in detail.

The graphene field effect transistor characteristics with temperature dependence were studied in the chapter 8. These devices were patterned using mechanical exfoliation method followed by photolithographic techniques.

In final, the synthesis of graphene oxide (GO) nano particles is explained in the chapter 9. In addition, the electrical transport of GO thin films was investigated in which low temperature properties are also given. The characterization techniques like XRD, UV-Vis, FT-IR and SEM analysis are also included in this chapter. The field effect transistor characteristics of GO thin film devices are also reported in this chapter.

# Chapter 1

## Introduction

### 1.1 Carbon Family - a brief

Carbon possesses a very particular position in the classification of the elements: indeed, it is the head of the central column of the periodic table. And this 14<sup>th</sup> column appears in fact as the spine of the classification. Its electro-negativity is medium, and during the chemical reactions, it can be as well electron donor as electron acceptor, according to the cases.

On the other hand, it exhibits a very large ability to create some chains by bonding with itself. It is well known that the organic chemistry is born for from this remarkable property. But it exists also some important consequences of this latter in the field of the inorganic chemistry. Indeed, the extreme variety of its allotropy is partly due to this property. It is due also to the ease for the carbon atom to change hybridization:  $sp^3$ ,  $sp^2$ ,  $sp$ , and even in some cases  $sp^x$  with  $x$  included between 2 and 3. (Figure. 1)

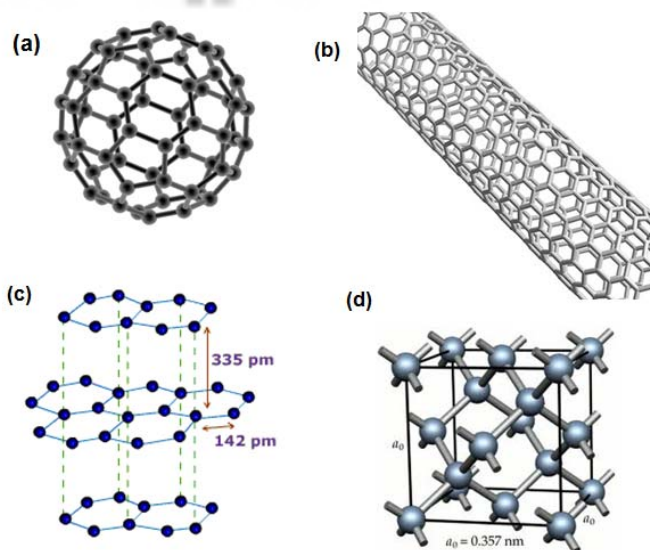


Figure. 1. Allotropy of carbon materials: (a) fullerene, (b) nanotube, (c) graphite and (d) diamond



The elemental solids obtained from  $sp^3$  carbon atoms are diamond (cubic variety) or more rarely lonsdaleite (hexagonal variety). Both materials are three-dimensional, because they exhibit strong covalent bonds that grow to infinity in the three directions of the space. But, in the room conditions, the thermodynamically most stable carbon material is graphite that appears as a lamellar solid (see Figure 1 c). It is built from  $sp^2$  carbon atoms and it is two-dimensional, because its covalent bonds grow to infinity in two directions of the space only: indeed the graphene planes are of course covalent structures, but they are stacked along the third axis by the means of very weak Van der Waal's bonds. One knows two graphite varieties: the hexagonal one, whose stacking is ABABAB..., and the rhombohedral one with an ABCABC... stacking. The first one is slightly more stable than the second one. With  $sp$  hybridization, the carbon atoms lead to several one-dimensional solids called choaites. They exhibit a fiber structure, since their covalent bonds grow to infinity in an unique direction of the space only. These linear covalent structures are gathered in beams. All these carbon materials can be observed in nature, but the choaites are however particularly rare, due to their weaker thermodynamical stability.

Several other carbon materials derive from distorted graphene planes. Indeed, a perfect graphene plane is strictly flat, but if several hexagons are replaced by pentagons, it becomes convex and can turn into a closed structure. For this reason, it is admitted that the carbon hybridization in this case is included between 2 and 3. Thus, this phenomenon generates the class of fullerenes; among with the roughly spherical (truncated icosahedron)  $C_{60}$  molecule is the best known. Using Van der Waal's bonds, the assembly of numerous  $C_{60}$  molecules leads to a cubic solid that appears as zero-dimensional, because its covalent bonds do not grow in any direction. This material is called fullerite and it is of course rather volatile, because it contains rather small molecules linked by Van der Waal's bonds.

Lastly, it is also possible for a graphene plane to wind around itself, after having suffered a more or less important torsion, leading to a cylindrical structure. These objects constitute the class carbon nanotubes. They can be single-walled (the cylinder is unique) or multi-walled (several cylinders are fitted together) and they are associated within beams generated by Van der Waal's bonds. Of course, these carbon nanotubes, whose diameter is nanometric, appear as one-dimensional



materials. Save the 3D diamond structure, all these carbon materials are anisotropic and exhibit Van der Waal's bonds that appear as weak points concerning the cohesion of these solids. Soft chemical reactions can exist for the latter, because, in these cases, the chemical reagents attract exclusively the areas of weak cohesion of the materials (often called Van der Waals's gaps), without disrupting their covalent parts.

## 1.2. Electronic Structure and Properties of Graphite

Graphite appears as the most stable carbon variety in room conditions. The  $sp^2$  hybridized carbon atoms that form the graphene planes are closely bound one another by means of very strong covalent bonds, whose length reaches 142 pm, and energy 25 eV/mole. The strength of these bonds is revealed also by a very high sublimation point of about 3700 K. In this 2D structure, each carbon atom is associated with three coplanar neighbors, so that the value of the C-C-C angles is exactly  $120^\circ$ , accordingly to the  $sp^2$  hybridisation. The unused  $p_z$  orbital of each carbon can build with neighbouring atoms  $\pi_z$  molecular orbitals that are of course delocalized on the whole of the graphene plane, as they are also in the case of the flat benzene molecule.

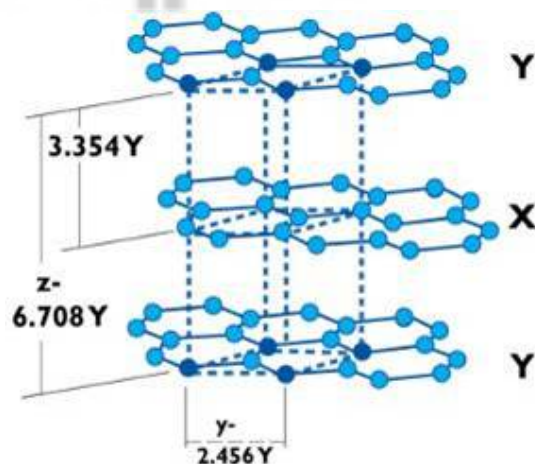


Figure.2. Crystal structure of hexagonal graphite

On the other hand, very weak Van der Waal's bonds provide the cohesion between the successive graphene planes that are stacked up into graphite. For this reason, two successive graphene layers in graphite are 335 pm apart. But they are not exactly

superimposed and their stacking corresponds to the ABAB.... sequence. The unit cell is hexagonal with the following parameters:  $a = 244 \text{ pm}$  and  $c = 670 \text{ pm}$  (ref. Figure. 2). This structure confers a very strong 2D character on graphite. It is a perfect example of lamellar material, whose sheets are monolayered. Its anisotropy appears in all fields. Its mechanical properties for instance exhibit a very good aptitude for the cleavage, so that graphite appears as a material often used in lubricating (oils, pencil lead, etc.). Similarly, its electrical properties are very anisotropic: graphite is indeed a poor conduction along the  $c$ -axis and it is much better conductor in the other directions, since the corresponding resistivities reach respectively  $0.1 - 1 \Omega\text{-cm}$  and  $40 \mu\text{-}\Omega\text{-cm}$ .

Graphite can be either natural or synthetic. Well crystallized natural graphite platelets principally, come from Madagascar, Sri Lanka, URSS or China. They are often mixed with other minerals like calcite or quartz and they have to be chemically purified after a manual sorting. Powder of synthetic graphite is obtained from pyrolysis of organic precursors followed by a step of graphitization. The ability of carbon to graphitize is determined during the pyrolysis. Hard carbon that is not graphitizable comes from carbonization without passing through a liquid phase.

It is also possible to prepare pyrolytic graphite. A carbon deposit on a heated graphite substrate is obtained by cracking of gaseous hydrocarbide diluted in argon. Graphitic sheets are parallel to the surface and when this pyrographite is heated at very high temperature ( $3000 \text{ }^\circ\text{C}$ ) under high pressure, the anisotropy of the material is increased and it becomes "highly oriented pyrographite" or "HOPG" whose properties are very close to those of a single crystal. In "HOPG", the  $c$ -axis of all crystallites, that are perpendicular to the graphene sheets, are parallel between them, with a maximal defect of  $1^\circ$ . However, the  $a$  and  $b$  axis are randomly oriented in the graphitic layers so that a HOPG platelet can be considered as a single crystal in the  $c$ -axis and as a powder in the perpendicular plane.

### 1.2.1 Properties of Graphite

Following are some graphite properties based on its structure and occurrence in nature.

### **Physical State**

The mineral graphite is steel gray to black in color and is odorless (Figure. 3). It is opaque and has a sub metallic luster. Graphite is very soft and has a greasy texture. It can be broken easily and leaves a black streak on the hand when touched. Although graphite is soft and flexible, it is not elastic in nature.



Figure. 3. Graphite crystal

### **Structure**

Graphite is crystalline in nature, however, perfect crystals of graphite are rarely found. The carbon atoms in graphite are arranged in a hexagonal manner in a planar condensed ring system. This gives the graphite crystals, a hexagonal shape. Different layers of graphite are stacked together and held by weak covalent forces, to form a giant covalent structure.

### **Melting Point**

Graphite has a high melting point above 3000° C, like that of diamond, the other allotrope of carbon. Hence, it is stable over a wide range of temperatures.

### **Density**

As there is a lot of vacant space between the graphite sheets, held by the weak covalent bonds, the density of graphite is 2.09 to 2.33 g/cc, which is lower than that of diamond. The measured specific gravity of graphite is approximately 2.26 g/cc, however, it depends upon the purity of graphite. Graphite with a higher ash content shows a specific gravity higher than 2.26, while natural graphite has a lower specific gravity or density due to the trapped porosity.

### **Solubility**

Graphite is insoluble in water as well as other organic solvents. There are no attractive forces that occur between the solvent molecules and the carbon atoms in graphite and so it fails to dissolve in any of the organic solvents.

### **Electrical Conductivity**

There is vast delocalization of electrons within the carbon layers of graphite. The delocalized electrons are free to move and are able to conduct electricity, thus making graphite a good conductor of electricity.

### **Chemical Properties of Graphite**

Graphite is chemically inert to almost all chemicals. It burns completely, when heated in oxygen to form carbon dioxide. However, it fails to burn in air, even if it is heated to high temperatures. When heated in the presence of concentrated sulfuric acid and potassium dichromate, graphite gets oxidized to carbon dioxide. Due to its chemical inertness and stability at high temperatures, it is widely used as a refractory material.

### **Uses of Graphite**

- Manufacture of 'lead' used in pencils
- Refractories
- Steel making
- Lubricant
- Making electrodes
- Manufacture of polishes and paints
- Molds in foundry

This was all about graphite properties and its uses. The unique graphite properties are responsible for its use in a variety of applications.

## **1.3. Electronic Structure and Properties of Graphene**

Graphene consists of  $sp^2$ -bonded carbon atoms arranged in a honeycomb structure (ref. Figure 4) whose isolation was first succeeded in 2004 by Novoselov and Geim in Manchester University. It suddenly drew many scientific interests as

graphene has unique band structure, so-called Dirac cones, which was confirmed by the observation of the half-integer quantum-Hall effect in 2005. Graphene has now become one of the main research topics in condensed matter physics.

Graphene is a nano-material combining very simple atomic structure with intriguingly complex and largely unexplored physics. Since its first isolation about six years ago researchers suggested a large number of applications for this material in anticipation of future technological revolutions. In particular, graphene is considered as a potential candidate for replacing silicon in future electronic devices.

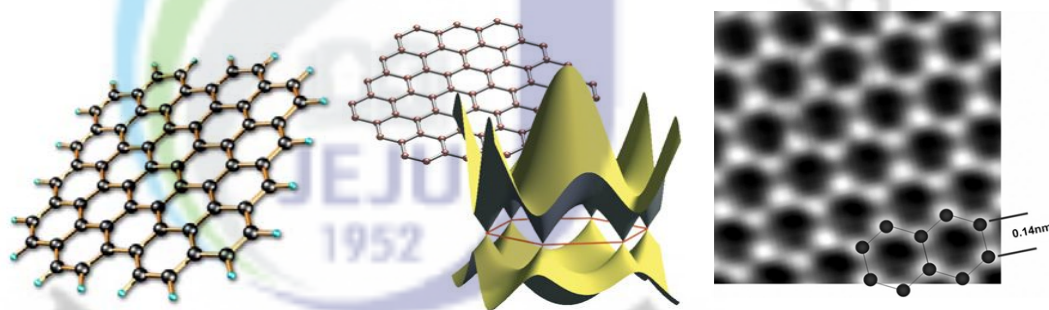


Figure 4. Monolayer sheet of carbon atoms (graphene) and its atomic structure (Hexagonal)

Graphene is a perfect example of the wonders of nanotechnology, in which common substances are scaled down to an atomic level to uncover new and exciting possibilities. Graphene is one of the strongest, lightest and most conductive materials known to humankind. It's also 97.3 percent transparent, but looks really cool under powerful microscopes.

### Graphene Fabrication

The most common method of graphene fabrication is exfoliation which finds its roots with a technique that has been around for centuries – writing with a graphite pencil. By writing with a pencil you create many graphene sheets spread over your paper. Unfortunately this method is uncontrollable and you are typically left with many sheets of varying thicknesses. If you want to study a single graphene sheet you need to locate it. The problem amounts to trying to find a needle in a haystack.



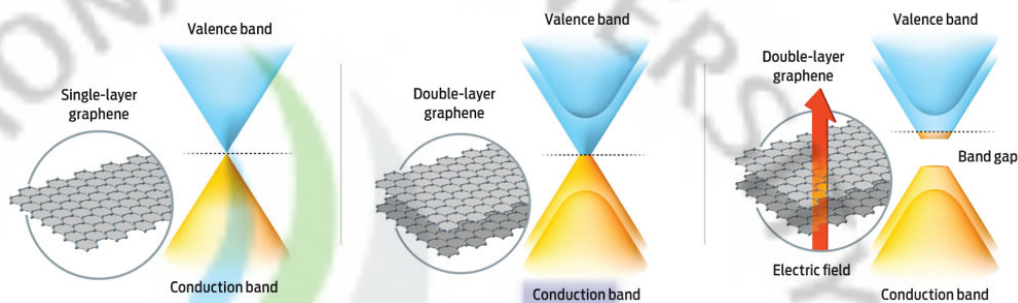


Figure. 5. Electronic structure of single, double layer graphene with and without electric field.

A way around this problem was solved by Andre Geim's group in Manchester (Novoselov, Geim et al. 2004). The general electronic structure of single layer and double layer graphene with and without electric field is shown in Figure. 5.

By gently rubbing or pressing a freshly cleaved graphite crystal on an oxidized silicon wafer graphene flakes with the correct thickness of oxide, single atomic layers are visible under an optical microscope due to thin film interference effects (Novoselov, Jiang et al. 2005; Blake, Hill et al. 2007). This technique simplifies the process of finding single graphene sheets but obviously limits this fabrication scheme to devices for research purposes. For the case of suspended graphene sheets as discussed in this thesis, this process may take  $\sim 1$  hour to find relatively thin  $\sim 1$ -5 nm thick suspended graphene devices but could take several days or weeks to find a suitable single suspended layer.

There are recent attempts to improve the quality and yield of exfoliation techniques. These include stamping methods which use silicon pillars to transfer graphene flakes and electrostatic voltage assisted exfoliation which uses electrostatic forces to controllably separate graphene from bulk crystals (Liang, Fu et al. 2007; Sidorov, Yazdanpanah et al. 2007). These are very recent developments and only time will tell whether they yield significant improvement over standard exfoliation. Another common graphene fabrication technique is to disperse graphene from solution. In this method graphite flakes are sonicated in a solution and then dispersed onto a wafer. An AFM is used to locate individual sheets making this technique very time consuming relative to the optical detection scheme. Long sonication times are needed to break the graphite down and this typically results in small flakes.

Recently a similar technique was used to fabricate graphene ribbons with nm-scale widths (Li, Wang et al. 2008). One of the difficulties in dispersing graphene from solution is separating the layers without breaking them. A way around this is to intercalate the graphite and dissolve it in a solvent. When the intercalant dissolves it separates the graphene sheets. This technique was shown to work effectively for graphene oxide. However, the success of similar techniques on graphene is limited due to the chemistry required to keep individual graphene sheets from aggregating in solution.

The technique which currently seems to have the greatest potential for mass production is the direct growth of graphene. Typically this is accomplished by heating a SiC wafer which results in the partial graphitization of the upper layer (Berger, Song et al. 2004). However, controlling the number of layers as well as the grain sizes is difficult with this technique limiting the mobilities achieved so far with this form of graphene (Berger, Song et al. 2006). Furthermore, isolating single sheets is problematic and additional lithography is required to pattern electrostatic gates on top of the graphene. Making suspended mechanical structures from grown graphene has yet to be demonstrated.

Chemical vapor deposition (CVD) and molecular beam epitaxy (MBE) are two other potential routes to graphene growth. Carbon nanotubes and diamond are successfully grown using CVD and the preferred method of growth for high quality GaAs/AlGaAs heterostructures is MBE. For the time being, exfoliation remains the preferred method for most of the experimental research groups around the world. However as in diamond, wide spread applicability of graphene is limited by the crude and time consuming methods currently used to fabricate and isolate single graphene sheets. The research community is currently in need of a reliable and reproducible graphene fabrication method if graphene is ever to move beyond being a laboratory curiosity.

### **Electronic Properties of Graphene**

Most of the experimental research on graphene focuses on the electronic properties. The most notable feature about the early work on graphene transistors was the ability to continuously tune the charge carriers from holes to electrons. An



example of the gate dependence in single layer graphene is shown in Figure. 6a. This effect is most pronounced in the thinnest samples whereas samples from multiple layers show much weaker gate dependence due to screening of the electric field by the other layers.

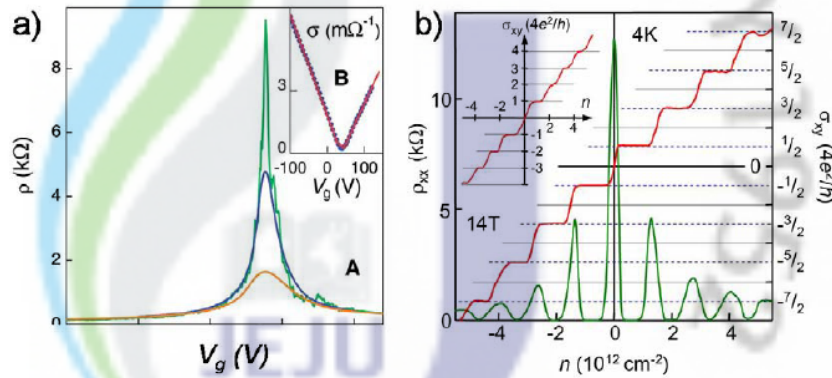


Figure. 6 (a) The resistivity of a single layer of graphene vs. gate voltage. (b) The Quantum Hall Effect in single layer graphene. Figures taken from (Novoselov, Geim et al. 2005)

At low temperatures and high magnetic fields, the exceptional mobility of graphene allows for the observation of the quantum hall effect for both electrons and holes (Figure. 6 b)(Novoselov, Geim et al. 2005; Zhang, Tan et al. 2005). Due to its unique band structure, the graphene quantum Hall effect exhibits a subtle difference from the conventional quantum Hall effect in that plateaus occur at half integers of  $4e^2/h$  rather than the typical  $4e^2/h$ . For more practical applications one would like to utilize the strong gate dependence of graphene for either sensing or transistor applications. Unfortunately, graphene has no band gap and correspondingly resistivity changes are small. Therefore, a graphene transistor by its very nature is plagued by a low on/off ratio. However one way around this limitation, is to carve graphene into narrow ribbons. By shrinking the ribbon the momentum of charge carriers in the transverse direction becomes quantized which results in the opening of a band gap. This band gap is proportional to the width of the ribbon. This effect is pronounced in carbon nanotubes where a nanotube has a band gap proportional to its diameter. The opening of a band gap in graphene ribbons has recently been observed in wide ribbon devices lithographically patterned from large graphene flakes (Han,

Ozyilmaz et al. 2007) and in narrow chemically synthesized graphene ribbons (Li, Wang et al. 2008).

## **Applications of Graphene:**

### ***Super-Small Transistors***

The Manchester team in 2008 created a 1-nanometer graphene transistor, only one atom thick and 10 atoms across. This is not only smaller than the smallest possible silicon transistor; Novoselov claimed that it could very well represent the absolute physical limit of Moore's Law governing the shrinking size and growing speed of computer processors.

### ***Super-Dense Data Storage***

Researchers around the world have already put graphene to work. A Rice University team in 2008 created a new type of graphene-based, flash-like storage memory, more dense and less lossy than any existing storage technology. Two University of South Florida researchers earlier this year reported techniques to enhance and direct its conductivity by creating wire-like defects to send current flowing through graphene strips.

### ***Energy Storage***

The energy applications of graphene are also extraordinarily rich. Texas's Graphene Energy is using the film to create new ultra-capacitors to store and transmit electrical power. Companies currently using carbon nanotubes to create wearable electronics – clothes that can power and charge electrical devices - are beginning to switch to graphene, which is thinner and potentially less expensive to produce. Much of the emerging research is devoted to devising more ways to produce graphene quickly, cheaply and in high quantities.

### ***Optical Devices: Solar Cells and Flexible Touchscreens***

A Cambridge University team argues in a paper in September's *Nature Photonics* that the true potential of graphene lies in its ability to conduct light as well as electricity. Strong, flexible, light-sensitive graphene could improve the efficiency

of solar cells and LEDs, as well as aiding in the production of next-generation devices like flexible touch screens, photo-detectors and ultrafast lasers. In particular, graphene could replace rare and expensive metals like platinum and indium, performing the same tasks with greater efficiency at a fraction of the cost.

### ***High-Energy Particle Physics***

In pure science, according to Geim, graphene “makes possible experiments with high-speed quantum particles that researchers at CERN near Geneva, Switzerland, can only dream of.” Because graphene is effectively only two-dimensional, electrons can move through its lattice structure with virtually no resistance. In fact, they behave like Heisenberg’s relative particles, with an effective resting mass of zero. It’s slightly more complicated than this, but here’s a quick and dirty explanation. To have mass in the traditional sense, objects need to have volume; electrons squeezed through two-dimensional graphene have neither. In other words, the same properties that make graphene such an efficient medium for storing and transmitting energy also demonstrate something fundamental about the nature of the subatomic universe.

## **1.4. Electronic Structure and Properties of Graphene-oxide**

Graphene oxide, a single-atomic-layered material made by reacting graphite powders with strong oxidizing agents, has attracted a lot of interest from scientists because of its ability to easily convert to graphene - a hotly studied material that scientists believe could be used to produce low-cost carbon-based transparent and flexible electronics.

Graphene oxide has been largely described as hydrophilic, or attracted to water. Graphene oxide sheets stabilized organic solvent droplets in water. (Credit: Image courtesy of Northwestern University). The electronic structure of graphene oxide and its AFM image are shown in Figure. 7. We can see in this figure, many functional groups like carbonyl, carboxyl, and hydroxyl groups are attached in its basal plane and its edges.

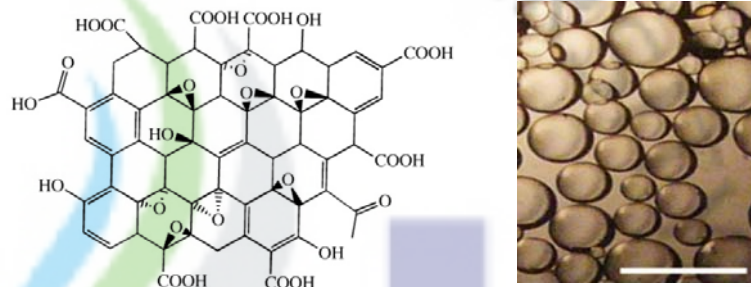


Figure. 7 The electronic structure of graphene oxide and AFM image of GO

### 1.5. Necessity for Development of Nanoscale of Graphitic Devices

In recent days, the micro/nano machining becomes an important process to fabricate micro/nano scale dimensional patterns or devices for many applications, especially in electrical and electronic devices. There are two kinds micro-machining in use. i) bulk micro-machining, ii) surface micro-machining. In the case of bulk micromachining, the structures can be made by etching inside a substrate selectively, however, in the case of surface micromachining; the patterns can be made on the top a desired substrate. FIB machining is considered as a one of famous bulk micro-machining processes. Many fabrication methods have been applied to fabricate the devices with smaller sizes [1-3], however, until now the size of the smallest pattern was only  $2 \times 2 \mu\text{m}^2$  was achieved with a lithography technique [4]. As an alternative approach, focused-ion-beam (FIB) etching technique is the best choice for the micro/nano scale patterning. FIB 3-D etching technology is now emerged as an attractive tool for precision lithography. And it is a well recognized technique for making nanoscale stacked-junction devices, nano-ribbons and graphene based 3-D Single Electron Transistor (SET) devices and their transport characterization studies.

FIB micro/nano machining is a direct etching process without the use of masking and process chemicals, and demonstrates sub-micrometer resolution. FIB etching equipments have shown potential for a variety of new applications, in the area of imaging and precision micromachining [5-6]. As a result, the FIB has recently become a popular candidate for fabricating high-quality micro-devices or high-precision microstructures [7]. For example, in a micro-electro-mechanical system (MEMS), this processing technique produces an ultra micro-scale structure

from a simple sensor device, such as, the Josephson junction to micro-motors [8]. Also, the FIB processing enables precise cuts to be made with great flexibility for micro- and nano- technology. Also, the method of fabricating three-dimensional (3-D) micro- and nano-structures on thin films and single crystals by FIB etching have been developed in order to fabricate the 3-D sensor structures [9-10].

The layered structure materials like graphite, Bi-2212, YBCO are recently attracted the world scientific community due to their interesting electrical and electronic properties reported in recent reports [11-12] for fabricating nanoscale devices, recently few interesting reports published on this material. In case of graphite, it is considered as a well known layered-structured material in which carbon sheets are arranged in a stacked-manner with interlayer distance of 0.34 nm. Each single graphite sheet is known as a graphene layer which is now becoming as one of hot topic in the world scientific community with lot of interest. Particularly the transport across the graphitic plane (along c-axis) is still unexplored well which need to be studied well. Our study on this research may open road to develop further graphite based electronic devices in which the unexplored properties of graphite nano-devices fabricated using FIB micro/nano machining technology could be possible to be explored.

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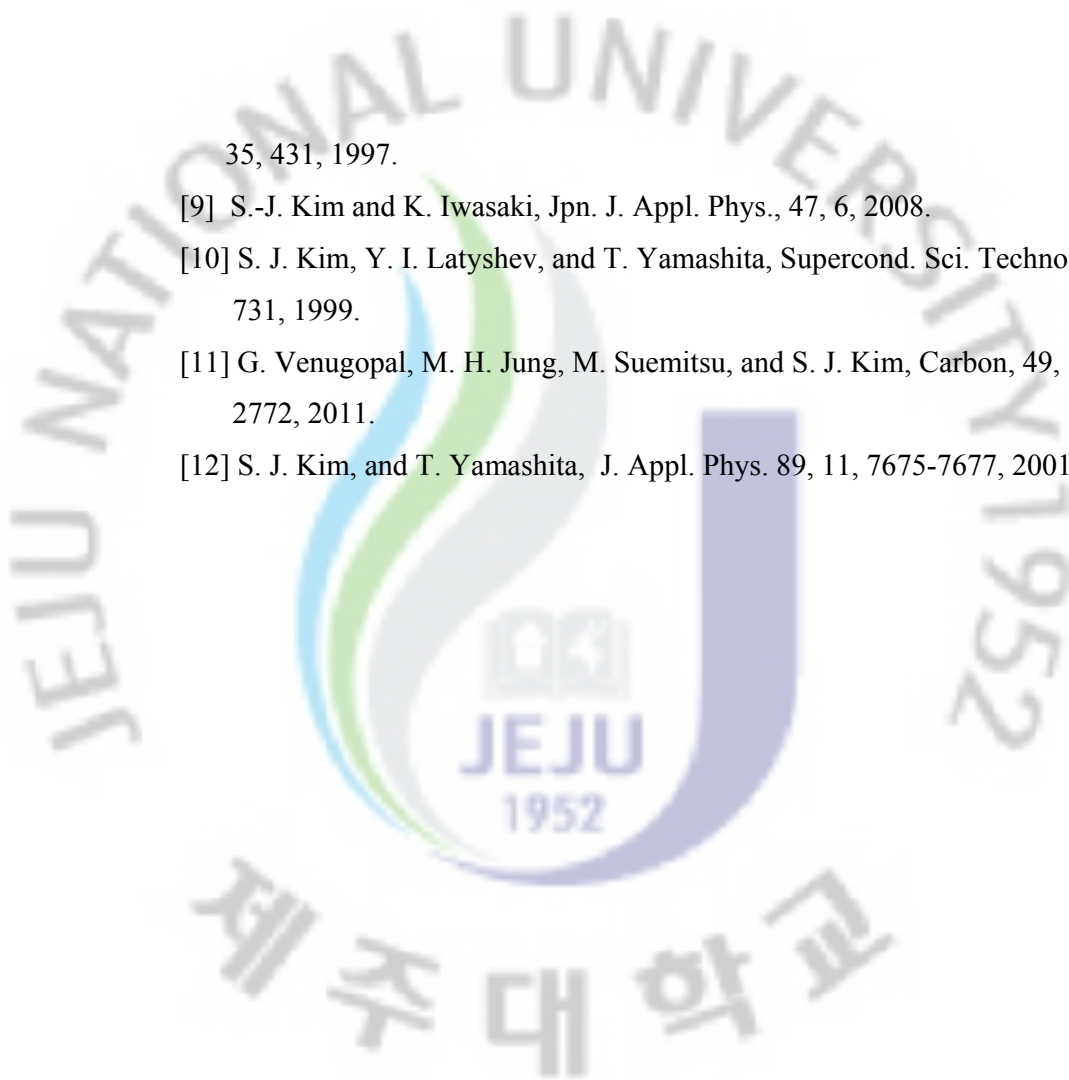
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## Chapter 2

# Experimental Techniques for Graphitic Nano-Device Fabrication

### 2.1. Introduction

This chapter provides detailed information on the experimental techniques used for the development of nanoscale graphitic devices in this work. The focused ion beam (FIB) three-dimensional technique used for nano-fabrication of graphite based nanoscale stacked-junctions. Mechanical exfoliation technique is used to prepare thin graphene flakes and the photo-lithography was used to make electrode pattern on the graphene layers. Further thermal evaporation and lift-off processes were followed for the graphene device fabrication, which are discussed in detail.

In addition, the synthesis of graphene oxide nanoparticles and GO thin film formation techniques are discussed in this chapter.

### 2.2. Focused Ion Beam 3-D Fabrication Technique

Miniaturization is the central theme in modern fabrication technology. Many of the components used in modern products are becoming smaller and smaller. Here, the focused ion beam (FIB) direct milling technique will be discussed with the focus on fabricating devices at the micrometer to nano-scale level. Because of the very short wavelength and very large energy density, the FIB has the ability for direct fabrication of structures that have feature sizes at or below 1  $\mu\text{m}$ . As a result, the FIB has recently become a popular candidate in making high-quality microdevices or high-precision microstructures.

The FIB has been a powerful tool in the semiconductor industry mainly for mask repairing, device modification, failure analysis and integrated circuit debugging. Two basic working modes, ion beam direct write and ion beam projection have been developed for these applications. The ion beam direct write process, also known as FIB milling (FIBM), is the process of transferring patterns by



direct impingement of the ion beam on the substrate. It is a large collection of microfabrication techniques that removes materials from a substrate and has been successfully used for fabricating various three-dimensional (3D) micro structures and devices from a wide range of materials. For the ion beam projection process, a collimated beam of ions passes through a stencil mask and the reduced image of the mask is projected onto the substrate underneath. The ion beam projection process is also known as focused ion beam lithography (FIBL) and can serve as an alternative to conventional optical lithography.

To develop the graphite stacked-junctions, planar-type nanostructures, we used a high-resolution FIB instrument (SII SMI-2050) which is shown below. The photo-image of FIB unit and the schematic of FIB functions are presented in Figure.

1.

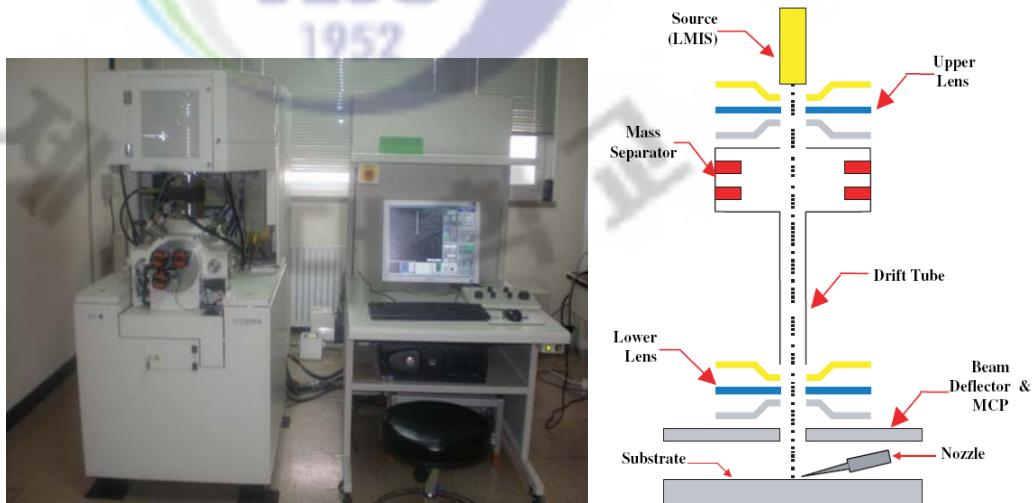


Figure. 1 The photograph image of our FIB unit and schematic of FIB machine parts.

In this project, we followed the 3-D etching technique by tilting the substrate stage up to  $90^\circ$  automatically for etching thin graphite flake. We have freedom to tilt the substrate stage up to  $60^\circ$  and rotate up to  $360^\circ$ . The steps of the fabrication process using a FIB etching are shown in Figure. 2 (a–d). The clear axes of the FIB process configurations with in-plane ( $x$ – $y$ ) and vertical axes (as  $z$  direction) are indicated in an axis diagram in Figure. 2(b). The in-plane area was defined by tilting the sample stage by  $30^\circ$  anticlockwise with respect to the ion beam and milling along the  $ab$ -

plane. The in-plane etching process is shown in Figure. 2(a)-(c). The out of plane or the c-axis plane was fabricated by rotating the sample stage by an angle of  $180^\circ$ , then tilting by  $60^\circ$  anticlockwise with respect to the ion beam, and milling along the c-axis direction. The schematic diagram of the fabrication process for the side-plane is shown in Figure. 2(d).

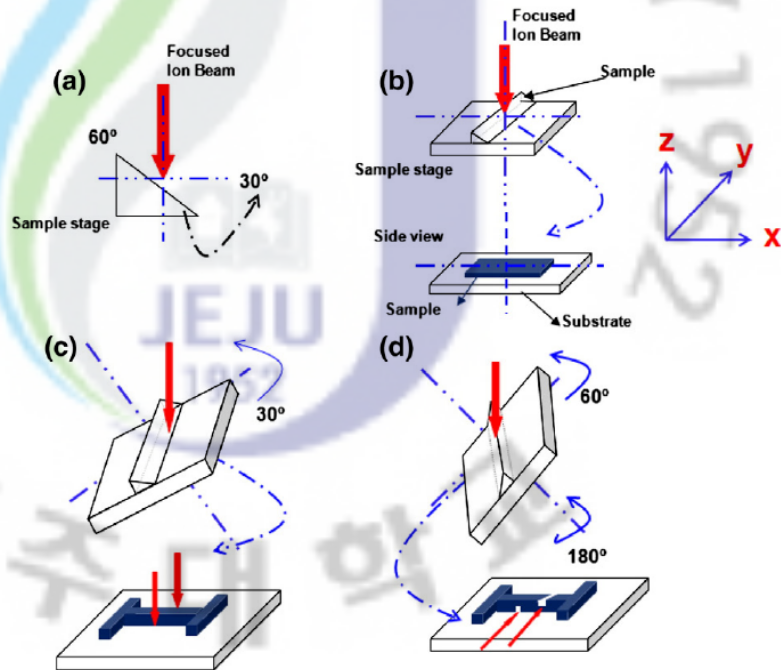


Figure 2. Nanoscale stack fabrication process using focused ion beam 3D etching method. (a) Scheme of the inclined plane has an angle of  $60^\circ$  with ion beam (where we mount sample). (b) The initial orientation of sample and sample stage. (c) Sample stage titled by  $30^\circ$  anticlockwise with respect to ion beam and milling along  $ab$ -plane. (d) The sample stage rotated by an angle of  $180^\circ$  and also tilted by  $60^\circ$  anticlockwise with respect to ion beam and milled along the c-axis.

By varying the stack height length and in-plane area, we can fabricate various sizes of stacked-junctions on the graphite layer. The number of elementary junctions in the stack will vary depends on the height of the junction. If junction height is more, the more number of elementary junctions exists which provide larger more resistance in c-axis characteristics.

The electrical transport characteristics were performed for this stack using closed-cycle refrigerator systems (CKW-21, Sumitomo) at various temperatures from 25 to 300 K with the use of the Keithley 2182A nanovoltmeters and source meters (6221) interfaced with Lab view software. The standard Keithley 2182A nanovoltmeter and source meter (6221) were used for this measurement. The models 2182A and 6221 are easy to use because the combination can be treated as a single instrument. Their simple connections eliminate the isolation and noise current problems. To obtain lower noise in the measurement data, we have also used a low-pass filter circuit in our measurement setup. These instruments were optimized to make low noise measurements at high speeds, typically just 15 nV p-p noise at 1 s response time, and 40–50 nV p-p noise at 60 ms. The observed output voltage was larger than the typical noise level of the instrument which proved that the measured data neither originated from measurement error nor from noise of instrument.

### **2.3 Mechanical Exfoliation Technique**

Graphite consists of a stack of many graphene layers with Van der Waals interlayer force of attraction. Since the Van der Waals force is weakest, graphite can be easily cleaved. For example, whenever using a pencil, one generates lots of graphene layers on papers without being noticed. By using this property, it is now possible to deposit graphene sheets on a desired substrate.

Steps for the mechanical exfoliation process from graphite to graphene. The sequence is listed below;

1. Stick a piece of natural graphite to 3M Scotch tape

Carefully select the graphite with a large flat surface. In addition to 3M Scotch tape Nitto tape can also be used, and it generally produces less glue on the substrate at the end of the process.

2. Cleave graphite in several times ( more than 30 times)

- Attach a tape on top of graphite surface and rub it gently.

- detach the tape gently.

- Inspect thickness of graphene flakes left on the tape by looking them through the bright light.

- Repeat the process until large enough thin graphene flakes remains on the tape.

3. Exfoliate graphene flakes on the substrate

Attach a tape with few graphite layers on top of the clean target substrate.

Rub it gently for 5-8 mins. We should note here, as the rubbing force increases, the rubbing time decreases. It depends on the people and the environment, but to get large area graphene, gentle rubbing for a long time is usually better.

- Detach a tape slowly from the surface of the substrate.

4. Search desired graphene sheets under the optical microscope

Thickness of graphene layers remained on the substrate can be identified by the optical microscope by a difference in colors or contrasts with visibility depending on the different kinds of the substrate. Commonly, highly doped silicon substrate with a 300-nm-thick SiO<sub>2</sub> layer is used. Usually, the magnification  $\times 200$  is enough to search graphene sheets.

By using this method, we can usually get 25-100  $\mu\text{m}$  sized graphene sheet, and in general, the larger graphite and the less cleaving processes produce the larger graphene sheet on the substrate.

## 2.4 Photolithography

As mechanically exfoliated graphene sheets are in a mesoscopic scale, a lithographic technique is required to make metallic contacts on the sheet. We use photo-lithography in this work to make electrode pattern. Details about the lithography process are discussed below. Figure 3 shows the mask aligner system which we used.



Figure. 3 Mask aligner system (MDA-400 M) for lithography pattern fabrication

The various stages of this lithography process or the procedures which we followed for lithographic pattern are given below:

**Stage -1 Wafer or substrate cleaning:**

- Use clouse in the entire experiment
- Use Iso-propyl alcohol to clean wafer/substrate
- Use DI water to clean
- Use tissue paper and Air - drying to remove the water particles from the surface of wafer (both side).

**Stage – 2 Spin coating of photo-resist :**

- The cleaned wafer to be put in spin coater and start creating vacuum
- Set spin coating rpm and time, using timer 1 and 2. (see the optimized parameter table)
- Put photo resist at the center of the cleaned wafer and spin coat.

**Stage – 3 Baking the wafer**

Put the spin coated wafer in the hot plate which is in 60° C for 150 sec and then remove wafer from the hot plate and do air cooling (only for back side of wafer )

**Stage – 4 UV Exposure**

Check and ensure the initial machine set up parameters is done carefully.

- Put the wafer on the substrate stage properly and press substrate Vac. button
- Put the mask in mask- holder and press Mask Vac. button on
- Mount the mask- holder over the substrate stage.
- Use Micrometer handle to bring the substrate stage and mask holder to touch each other. (no gap should be maintained between them). Be careful while doing this process.
- Press Vacuum contact button
- Then wait for 20 sec.
- Turn Align and Exposure knob one by one carefully.
- Now the aligner system will start working and comes to its position.
- Set the expose time by using timer (standard 2.5 sec).
- Now press Exposure button.
- After exposing UV light, turn off align and exposure knob.



### **Stage – 5 Removal of wafer**

- Now put off Vacuum contact button
- Then bring down the stage by using Micrometer handle
- Remove mask holder carefully
- Then press substrate vac. button off and remove wafer from the wafer stage.

### **Stage – 6 Developing process**

The UV-exposed wafer to be put in developer solvent [we used standard developer solution AZ 300 MIF]. Slow soaking has to be performed with respect to user need and process. In this process, the UV-unexposed parts (in case of positive PR) the photo-resist will be dissolved in the developer solution and show clear electrode pattern we fabricated via mask. Then put the wafer in DI water bath for 1 min and do air- drying to clean the wafer thoroughly.

### **Stage – 7 Pattern Analysis**

**After developing,**

- Put the developed wafer again in wafer stage and press substrate Vac. Button
- Use CCD camera -module's adjusting knobs in order to check the developed pattern.

#### **Optimized condition for Lithographic Process in MDA-400M Mask Aligner (using AZ 5214 positive photo-resist)**

Sample	Spin coating		Prebake		Expose UV with Mask	Developing time	Remarks
1	300 rpm 6sec (timer 1)	2200 rpm 40 sec (timer 2)	60°C	150 sec	55 sec	2 sec	Excellent 4-probe Pattern obtained

**After completing the experiment: Mask cleaning to be done**

Mask cleaning after exposure is important in the lithographic pattern process. Hence, we can avoid the defects deposited in mask during next experiment time.

To clean the mask, we need to follow the following:

- rinse the mask with acetone
- rinse the mask with IPA
- Dry the mask using the N2 gun

The schematic of the detailed lithographic process is presented in Figure.4 (a-e).



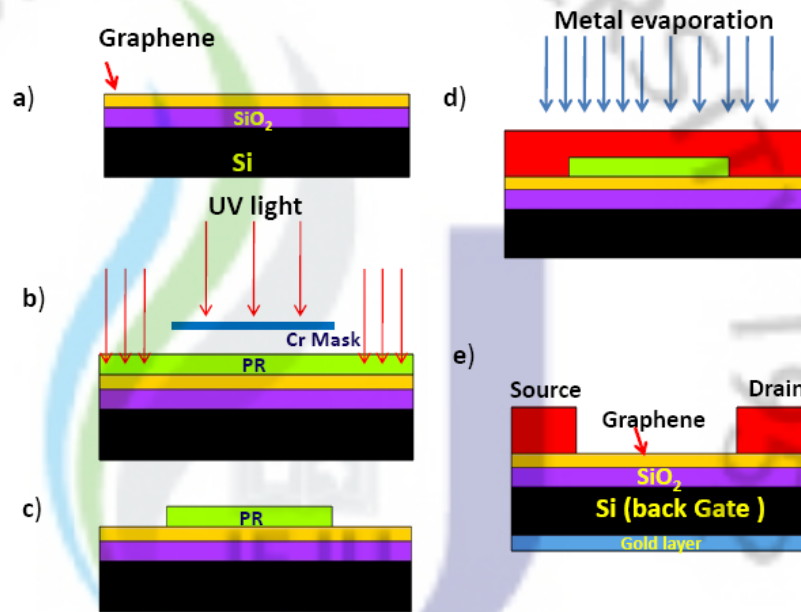


Figure. 4. Photolithographic process of electrode patterning on graphene. (a) Graphene flake on Si/SiO<sub>2</sub> substrate (b) Photoresist is spin-coated over the graphene flake and UV light illuminated through Cr mask. (c) the pattern after developing process (d) gold (Au) evaporation thro thermal evaporation technique (e) after lift-off process, the device with source and drain electrode structure with back-gate configuration.

After the lithography, metallic Au/Al electrodes are deposited by using thermal evaporation system. Then lift-off process is carried out (using acetone) to get the final pattern for device characterization. If necessary, graphene can be etched to a desired shape by the oxygen plasma ashing with negative or positive electron-beam resist stencils, which we have not followed in this work.

## 2.5 Modified Hummers method for graphene-oxide synthesis

The graphene oxide (GO) nanoparticles were synthesized by a modified Hummers method using expandable graphite powders as the starting material. Briefly, the expandable graphite powders (2 g) was stirred in 98% H<sub>2</sub>SO<sub>4</sub> (35 ml) for 2 h. KMnO<sub>4</sub> (6 g) was gradually added to this solution while keeping the temperature less than 20 °C. The mixture was then stirred at 35-40 °C for 30 min, and then at 65-

80 °C for 45 min. The resulting solution was diluted by adding 46 ml of water and the mixture heated at 90 °C for 30 min. The reaction was terminated by addition of 150 ml of distilled water and 30% H<sub>2</sub>O<sub>2</sub> solution (10 ml). The mixture was washed by repeated centrifugation with 5% HCl aqueous solution followed by deionized water until the pH of the solution becomes neutral. To obtain GO particles, 160 ml of water was added resulting precipitate and sonicated well to make a uniform suspension for graphene oxide.

## Chapter 3

### Study of Temperature Dependence of Planar-type Graphite Structures

In this chapter, we have discussed the temperature dependent transport behavior for the planar-type structures along *ab*-plane fabricated in micron-scale graphite layers. The planar-type structures of graphite layers were fabricated by using a focused ion beam (FIB) etching method. In-plane areas of  $10\ \mu\text{m} \times 10\ \mu\text{m}$ ,  $6\ \mu\text{m} \times 5\ \mu\text{m}$ ,  $6\ \mu\text{m} \times 2\ \mu\text{m}$ , and  $1\ \mu\text{m} \times 1\ \mu\text{m}$  exhibit semiconducting behavior which is contradictory to conventional metallic behavior of graphite flakes and show a small drop in resistance around 49 K. The origin of this effect is suspected from  $\text{Ga}^+$  ion damage during FIB fabrication. The fabricated planar-type structures show a transition in the current (*I*) - voltage (*V*) curves from diode-like characteristics around 30 K to an Ohmic behavior around 300 K.

### 3.1. Introduction

Currently, the research on carbon allotropes, like graphite, diamond, and Buckminster fullerenes ( $C_{60}$ ) have attracted more attention by physicists around the world due to their excellent unique properties on micro-electronic applications. Particularly, graphene becomes an active replacement material for silicon, which is being used heavily in semiconductor industries nowadays [1-2]. Relativistic Dirac theory predicted that charge carriers in graphene would have mass-less fermions which can travel thousands of lattice spacing without scattering [3-4].

Graphite consists of stacked layers of many graphene sheets held together by weak interlayer interaction forces [5]. Each sheet has a hexagonal lattice [6] of carbon bonded by strong  $\sigma$  bonding ( $sp^2$ ) in the  $ab$ -plane. The perpendicular  $\pi$ -orbital electrons along the  $c$ -axis are responsible for the  $ab$ -plane conductance [7]. The graphite crystallites with thicknesses ranging from 1 to 100 nm are typically prepared by synthesizing thin graphite layers directly on top of a substrate [8] or by extracting them using chemical [9] or mechanical [10-11] methods.

The studies on bulk graphite materials have been conducted for many years [12-13]; however, there has been no work done on thin graphite planar-type structures. The temperature dependence of the electrical transport measurements for these planar-type structures has not been measured because the geometry and the size of these structures are considered to be too small for these experiments. In futuristic electronics applications, we need to pay a special attention to two-terminal devices such as a Josephson junction diode [14]. Here, we report about the temperature dependence of graphite planar-type structures fabricated using FIB etching technique and their transport characteristics using two-electrode measurements. Also we describe a method used to extract thin graphite layers from a bulk highly-oriented pyrolytic graphite (HOPG) using 3M scotch tape.

### 3.2. Experiments

The Si/SiO<sub>2</sub> structures were used as substrates and were cleaned with acetone. The thickness of the SiO<sub>2</sub> layer on Si was approximately 300 nm. Then, the substrates were put in an ultrasonic bath for 15 min. We repeatedly peeled off the

surface layers of highly-oriented pyrolytic graphite (HOPG) material by using mechanical exfoliation method [15], and those separated layers were transferred to the Si/SiO<sub>2</sub> substrates. Thin graphite layers were identified by using an optical microscope. This process allowed us to prepare several samples in a matter of hours, which is the main advantage of this method. The sample reproducibility was quite good when using this method. The two electrodes were made with silver paste for the electrical measurements. We annealed the contacts at 300°C to decrease the contact resistance. The planar-type structures along *ab*-plane were fabricated on the graphite layer by using focused-ion-beam (FIB) 3-D etching technique as per the procedures followed in the section. 2.2. The thickness of graphite layer that we used for fabricating the planar-type structures was approximately 500 nm. These micro-fabrication etching methods are discussed in detail elsewhere [16, 17]. We fabricated 10 μm x 10 μm, 6 μm x 5 μm, 6 μm x 2 μm, and 1 μm x 1 μm planar-type graphite structures by using FIB (SII Inc. Model SMI 2050).

The electrical transport measurements of the planar-type graphite structures were carried out in a closed-cycle refrigerator (SUMITOMO, SRD 204). In Figure. 1, we show a FIB image of a fabricated 10 μm x 10 μm planar-type graphite structure (image scale bar is 20 μm).

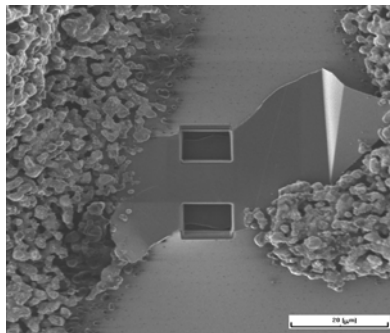


Figure. 1. FIB image of a 10 μm x 10 μm planar-type structure fabricated in a graphite layer with two-electrodes. (Scale bar is 20 μm)

The resistance (*R*) – temperature (*T*) characteristics of the planar-type structure are shown in Figure 2. The transport measurement was carried out from 300 K to 30 K. The in-plane resistance shows a gradual increase to a high resistance value of Mega



Ohms at 30 K. This exhibits a semiconductor-like behavior. This generation of high resistance is contributed by stronger boundary scattering in thinner samples [18].

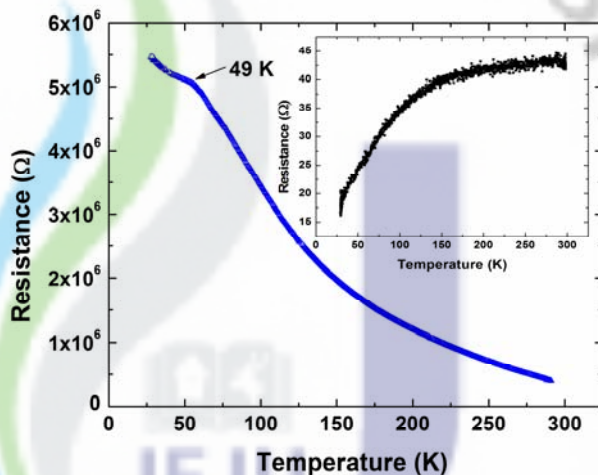


Figure 2.  $R$ - $T$  characteristics of a  $10\ \mu\text{m} \times 10\ \mu\text{m}$  planar-type structure showing a semiconductor-like behavior. The inset shows a metallic behavior for a bare graphite flake which have no planar-type structure.

A sufficient number of  $\pi$ -orbital electrons are not available in thinner layers which lead to poor conductivity. However, thicker flakes, which have no planar-type structures, show a metallic behavior, as shown in the inset in Figure 2. We also found a small drop in the resistance at 49 K. The reason for the resistance drop of 49 K is believed to be the onset of delocalization of charge carriers in the graphite layer at this temperature and/or electrode contact problem with graphite layer. Since graphite is considered to be a low-carrier-density, high-purity semimetal [5], we observed both a metallic nature for thicker flakes and a semiconductor-like behavior for the planar-type structures fabricated in thinner flakes, from the  $R$ - $T$  characteristics. We suspect that this semiconductor-like property can be possible to be originated from either contact-resistance of two-electrode measurement system or damage of graphite surface raised by the scanning of  $\text{Ga}^+$  ions from FIB. We observed similar semiconductor-like behavior for other planar-type structures,  $6\ \mu\text{m} \times 5\ \mu\text{m}$ ,  $6\ \mu\text{m} \times 2\ \mu\text{m}$ , and  $1\ \mu\text{m} \times 1\ \mu\text{m}$  which show small drops in the resistance at 54 K, 69 K, and 102 K, respectively. It shows that the temperature values at which the resistance drops varies with the area of the respective planar-type structures.

### 3.3. Results and Discussion

Figure 3 shows the  $I$ - $V$  characteristics of a  $10\ \mu\text{m} \times 10\ \mu\text{m}$  planar-type structure measured at 300 K and 30 K.

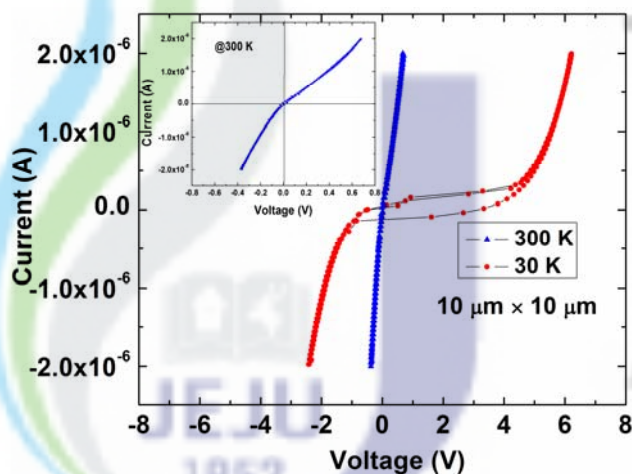


Figure. 3.  $I$ - $V$  characteristics of a  $10\ \mu\text{m} \times 10\ \mu\text{m}$  planar-type structure at 300 K and 30 K. At 300 K, an Ohmic behavior is observed. At 30 K, diode-like behavior is noticed. The inset shows  $I$ - $V$  characteristics at 300 K for the bare graphite flake which have no planar-type structure.

We observed an Ohmic behavior at 300 K and diode-like characteristics at 30 K. The inset shows an Ohmic behavior at 300 K for bare graphite flake which have no planar-type structure. Figure 4 shows the  $I$ - $V$  characteristics for a  $10\ \mu\text{m} \times 10\ \mu\text{m}$  planar-type structure at various temperatures. The temperature dependence of the planar-type structures shows asymmetric  $I$ - $V$  curves. Since these planar-type structures were fabricated along  $ab$ -plane, the  $\text{Ga}^+$  ions from FIB were possibly deposited over graphite surface which may stimulate larger resistance in transport measurements. Because of this resistance, the bias voltage gradually shifts to a higher value when the temperature decreases to 30 K.

We also observed similar behaviors in other planar-type structures with sizes of  $6\ \mu\text{m} \times 5\ \mu\text{m}$ ,  $6\ \mu\text{m} \times 2\ \mu\text{m}$ , and  $1\ \mu\text{m} \times 1\ \mu\text{m}$ . We have compared the  $I$ - $V$  characteristics of  $10\ \mu\text{m} \times 10\ \mu\text{m}$ ,  $6\ \mu\text{m} \times 5\ \mu\text{m}$ , and  $6\ \mu\text{m} \times 2\ \mu\text{m}$  planar-type structures measured at 30 K, which are shown in Figure. 5.

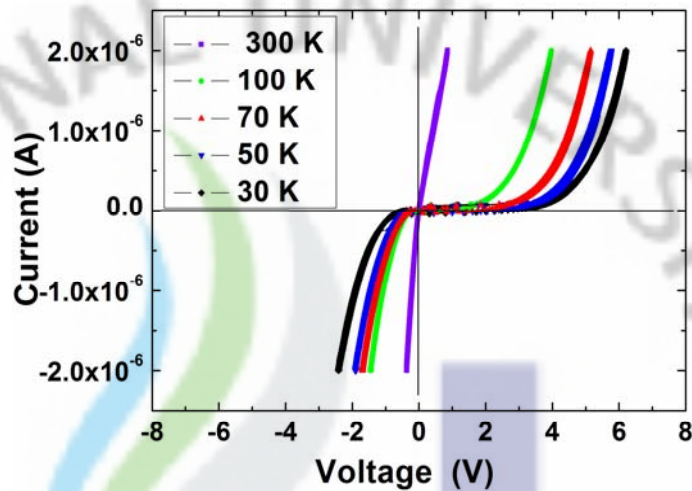


Figure 4.  $I$ - $V$  characteristics of a  $10\ \mu\text{m} \times 10\ \mu\text{m}$  planar-type structure measured at various temperatures. This shows asymmetric  $I$ - $V$  curves. The values of the forward and the reverse bias voltages shift to higher values gradually when the temperature is decreased to 30 K.

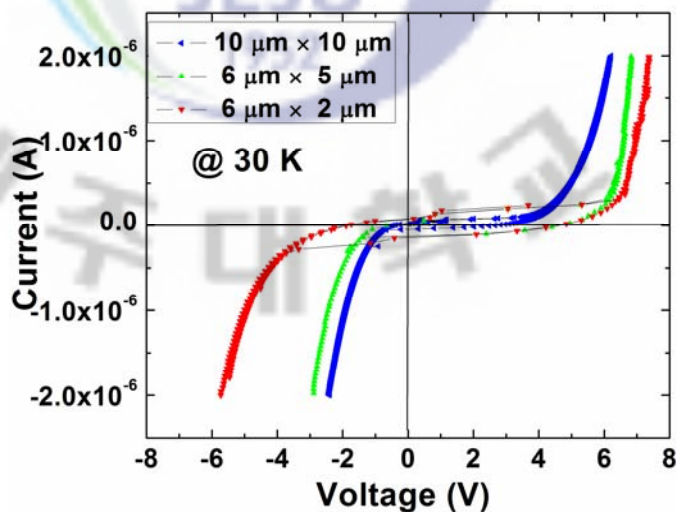


Figure 5. Comparison of the  $I$ - $V$  characteristics for  $10\ \mu\text{m} \times 10\ \mu\text{m}$ ,  $6\ \mu\text{m} \times 5\ \mu\text{m}$ , and  $6\ \mu\text{m} \times 2\ \mu\text{m}$  planar-type structures at 30 K.


We observed that while decreasing the fabrication size of planar-type structure, the value of forward bias voltage in the  $I$ - $V$  curve increases. This result reveals that a very small-sized fabricated planar-type structure restricts the flow of charge carriers more by providing large resistance.

### 3.4. Summary

In summary, we have characterized and reported the temperature dependence of transport characteristics of planar-type structures fabricated in graphite flakes by using the FIB etching technique. The fabricated planar-type structures have shown semiconductor-like characteristics. This is originated either from two-electrode system or the effect of  $\text{Ga}^+$  ion damage from FIB. The resistance drop at 49 K in the  $R$ - $T$  characteristics is believed to be due to an onset of the delocalization of charge carriers. The  $I$ - $V$  characteristics show a transition from diode-like characteristics at 30 K to an Ohmic behavior at 300 K. The size-dependent  $I$ - $V$  characteristics of planar-type structures were also discussed in which the smaller size among the fabricated structures has shown high resistance to charge carriers. Also, a clear asymmetry in  $I$ - $V$  curves was noticed for all these planar-type structures.

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## Chapter 4

### Fabrication and Characteristics of Large In-plane area Graphite Stacked-Junctions

In this chapter, we report about the fabrication and characteristics of planar-type micro-structures (having large in-plane area along  $ab$ -plane and  $c$ -axis) fabricated on thin graphite layer using a three-dimensional focused-ion-beam (FIB) etching technique. We have fabricated several in-plane area of sizes of  $6\ \mu\text{m} \times 6\ \mu\text{m}$ ,  $6\ \mu\text{m} \times 4\ \mu\text{m}$  and  $6\ \mu\text{m} \times 2\ \mu\text{m}$  planar-type micro-structures/patterns on thin graphite layer using FIB. The  $c$ -axis stack with the height of several nanometers was also fabricated. The transport characteristics were studied for these structures. We have observed a peculiar anomalous transition from ohmic behaviour to curve-like nonlinear characteristics below 110 K from current ( $I$ )-voltage ( $V$ ) curves for  $ab$ -plane and  $c$ -axis stack. A clear nonlinear characteristics has been observed at 25 K. Resistance versus temperature ( $R$ - $T$ ) and  $I$ - $V$  characteristics of the  $ab$ -plane and  $c$ -axis stack strongly resemble this anomalous-transition behaviour. These results show the superiority of graphite-microstructures for futuristic graphite-based nonlinear electronic devices.

## 4.1. Introduction

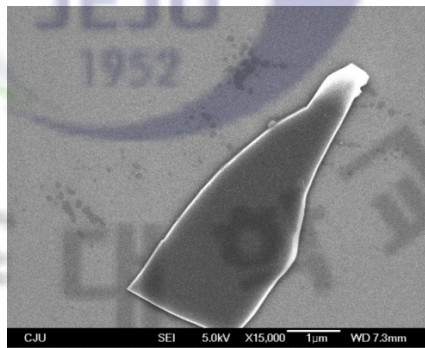
Even though a considerable amount of studies has been performed on graphite materials, their transport properties are still not well understood. Graphite is a three dimensional (3-D) material which has a sheet-like layered structure where the carbon atoms all lie in a plane and are only weakly bonded to the adjacent graphite sheets [1]. It is normally a basic material for all above carbon allotropes. Recently, the research on graphite materials such as two-dimensional graphene (single atomic layer of carbon), zero dimensional fullerenes ( $C_{60}$ ) and carbon nanotubes have attracted much attention by their unique properties for micro and nano-electronic applications. From bulk graphite, graphene (a one atomic thick layer) has recently cleaved and emerged as a fascinating material system for fundamental studies in condensed-matter physics [2, 3]. Particularly, graphene becomes an active replacement material for silicon which is being used heavily in semiconductor industries nowadays [4]. Each sheet has hexagonal lattice of carbon bonded by strong  $\sigma$  bonding ( $sp^2$ ) in the  $ab$ -plane. The perpendicular  $\pi$ -orbital electrons along the  $c$ -axis are responsible for  $ab$ -plane conductivity [5]. The scientific interest on graphite has been recently renewed by recent magnetization [6] and transport [7] results on highly oriented pyrolytic graphite (HOPG). In this chapter, we report a detailed fabrication technique for planar-type micro-structures on thin graphite layer and our observation of anomalous change of transport characteristics below 110 K for  $ab$ -plane and  $c$ -axis stack fabricated by using focused ion beam. In general, the electronic devices such as diodes, bipolar junction transistors (BJT's), and field effect transistors (FET's) are described in terms of their nonlinear  $I$ - $V$  curves. Recently, these devices have been developed with respect to low noise, low power, and high electron mobility transistor applications [8]. Their electronic transport properties present remarkable scientific and technological potential.

Although the studies on bulk graphite have been investigated for many years, there has been no work reported yet on the fabrication of planar-type micro-structures along  $ab$ -plane and  $c$ -axis on thin graphite layer using focused ion beam. In addition the observation of anomalous change in transport characteristics have not been ever reported elsewhere. Thus, our research has focused primarily on the

fabrication of micro-structures using FIB etching technique and studies on their anomalous transport characteristics.

## 4.2. Experiment Details

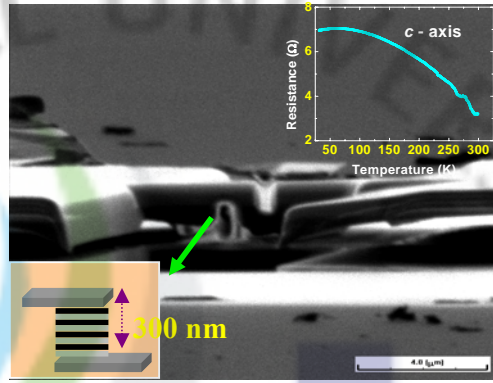
In this study, we used thin graphite crystallites extracted from highly ordered pyrolytic graphite (HOPG) using the mechanical exfoliation technique, as this method had been shown to form perfect crystallites [9]. Figure. 1 shows the SEM image of exfoliated graphite layer on Si/SiO<sub>2</sub> substrates. We have fabricated several planar-type micro-structures or patterns (along *ab*-plane and *c*-axis) on thin graphite layer (thickness ~ 500 nm) using FIB. Those in-plane area sizes were 6 μm × 6 μm, 6 μm × 4 μm and 6 μm × 2 μm.



**Figure. 1.** SEM image of a thin graphite flake on Si/SiO<sub>2</sub> substrate exfoliated from bulk graphite. (image scale bar is 1 μm).

We followed the FIB fabrication procedures as we mentioned in section 2.2. The fabricated *c*-axis stack size was  $W = 2 \mu\text{m}$ ,  $L = 1 \mu\text{m}$ ,  $H = 300 \text{ nm}$  which is shown in Figure. 2. The schematic picture of stack arrangement in graphite layer is shown as inset in Figure. 2.

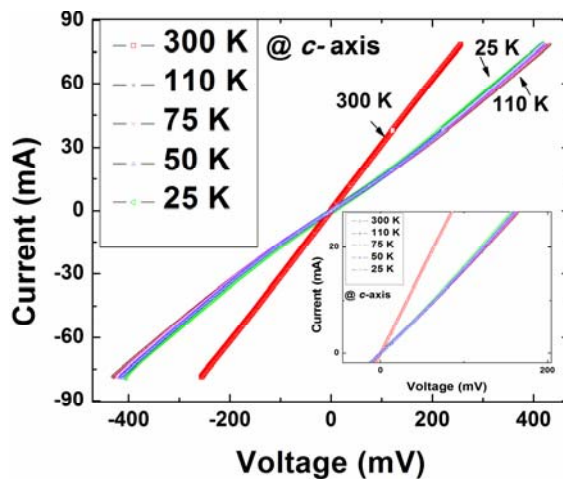
The electrical transport characteristics were performed for both *ab*-plane and *c*-axis stack micro-structures using four-probe contact measurement by using closed-cycle refrigerator system. These fabrication and etching details were reported in detail by Kim S J *et al* [10].



**Figure. 2.** The FIB image of *c*-axis stack fabricated on graphite layer. The stack size was  $W = 2 \mu\text{m}$ ,  $L = 1 \mu\text{m}$ ,  $H = 300 \text{ nm}$ . Inset (left bottom) shows the schematic diagram of stack arrangement along the *c*-axis. Inset (top right) shows the  $R$ - $T$  characteristics of *c*-axis stack.

### 4.3. Results and Discussion

The upper inset of Figure.2 represents the resistance ( $R$ ) – temperature ( $T$ ) characteristics of *c*-axis stack which shows semiconducting behavior till 50 K and then metallic behavior below 50 K. This is well agreed with previous theory reported by K. Matsubara *et al* [11]. Below 50 K, the impurity-assisted interlayer hopping conduction combined with scattering of carriers can be responsible for the metallic like behavior. Above 50 K, thermal excitation of carriers plays a major role for semiconductor-like temperature dependent behavior [12].

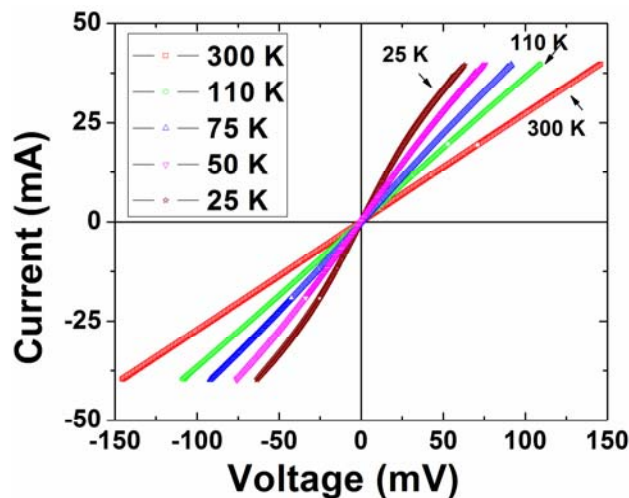


**Figure. 3.** The observation of nonlinear  $I$ - $V$  characteristics for *c*-axis stack fabricated on a graphite layer. The  $I$ - $V$  results of *c*-axis stack show a non-symmetric transition from linear to nonlinear behavior.

Most noticeably, we observed linear-ohmic behavior at 300 K and the same has been turned into nonlinear curve-like characteristics below 110 K from  $I$ - $V$  characteristics (ref. Figure. 3).

Below 110 K, there is no large shift in  $R$  value between the temperatures 110 K, 75 K, 50 K and 25 K. Hence these temperatures exhibit nonlinear characteristics all together with very low difference in  $R$  value. The inset shows a magnified region of nonlinear curve below 110 K since the voltage shift difference is found as minimum. As the  $c$ -axis stack consists of many elementary junctions along the  $c$ -axis, the nonlinear type  $I$ - $V$  curves of tunneling characteristics appear. However the fabricated in-plane structures exhibit a typical metallic behavior similar to the characteristics observed for bare graphite flake. Interestingly, we have noticed a kink-type structure in the  $R$ - $T$  curves between the temperatures 40 to 60 K for in-plane fabricated structures. The temperature where the kink-structure noticed is varied with respect to the sample resistivity. This small upturn in resistance at low temperature is not yet understood but it is either due to electrode contact or contact of electrode to the graphite flake. Also, we ensured that there is no substrate-induced effect behind this kink formation.

In Figure. 4. we show the  $I$ - $V$  characteristics of the  $6 \mu\text{m} \times 2 \mu\text{m}$  size planar-type structure. Similar to  $c$ -axis stack, the fabricated in-plane structures also shown a linear ohmic behavior at 300 K which turns into nonlinear behavior below 110 K.



**Figure. 4.** The  $I$ - $V$  characteristics of  $6 \mu\text{m} \times 2 \mu\text{m}$  size planar-type structure shows linear-ohmic behavior at 300 K and the same is turned into nonlinear curve-like characteristics at 25 K.



A clear nonlinear characteristic has been observed at 25 K. We describe this effect that below 110 K there is a possibility of rapid decrease in effective charge carriers which may stimulate the ohmic behavior into nonlinear characteristics. Most noticeably, a symmetricity in the  $I$ - $V$  curves has been observed. As the  $ab$ -plane and  $c$ -axis stack show their respective metallic and semiconducting transport characteristics, the transition from linear to nonlinear behavior in their  $I$ - $V$  curves clearly indicates their respective behavioral directionality. We observed similar characteristics as well for all other fabricated planar-type structures of sizes  $6\ \mu\text{m} \times 6\ \mu\text{m}$  and  $6\ \mu\text{m} \times 4\ \mu\text{m}$ . We also analyzed the size-dependent nonlinear characteristics in which the  $6\ \mu\text{m} \times 2\ \mu\text{m}$  size structure shows larger resistance when compared other fabricated sizes. A greater shift in bias voltage was observed in  $I$ - $V$  curve for the  $6\ \mu\text{m} \times 2\ \mu\text{m}$  size rather than the other sizes. The  $ab$ -plane and  $c$ -axis stack transport results were compared from which we declare that the  $c$ -axis stacks behave as a resistive-barrier to charge carrier tunneling. This is because of the high resistance generated by weakly bonded adjacent layers in the stack [1].

#### 4.4. Conclusion

Concluding, we successfully fabricated and characterized the planar-type microstructures fabricated on a thin graphite layer using FIB etching technique. We declare that we are the first to report out our observation of anomalous change of transport characteristics from ohmic to nonlinear behavior from  $I$ - $V$  characteristics. As the fabricated structures have lot of elementary junctions along the  $c$ -axis, the interlayer hopping conduction and thermal excitation of carriers play a key role for this effect. The main reason behind this effect is expected from either due to the decrease in number of effective charge carriers at that particular temperature or from the anisotropic thermal properties of the graphite. A detailed further investigation on this transition from linear to nonlinear behavior is required to understand these anomalous characteristics more clearly.

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Sugihara, K.: Phys. Rev. B 37, 4752 (1988)

## Chapter 5

### Temperature Dependence of Transport Anisotropy of Graphite Planar-type Structures

In this chapter, we report on the observation of temperature dependent anisotropic transport behavior for planar-type nanostructures (in-plane and out-of-plane) fabricated on thin graphite layer using a three-dimensional focused-ion-beam (FIB) etching technique. The transport characteristics were studied for several in-plane areas with sizes of  $6 \times 6 \mu\text{m}^2$ ,  $6 \times 4 \mu\text{m}^2$  and  $6 \times 2 \mu\text{m}^2$  planar-type structures/patterns and out-of-plane structures with the dimensions of  $2 \times 1 \times 0.3 \mu\text{m}^3$ . Both in-plane ( $\rho_a$ ) and out-of-plane ( $\rho_c$ ) resistivities are measured for these structures and the ratio of resistivity anisotropy is determined. The observed values of anisotropy ratio  $\rho_c/\rho_a$  were  $\sim 12.5$  at 300 K and  $\sim 54$  at 25 K. The room temperature value of  $\rho_c/\rho_a$  is varying by a few orders from the values of previously reported anisotropy results of bulk pyrolytic graphite. However, the value of resistivity anisotropy increases with decreasing temperature which is an identical behavior to the bulk pyrolytic graphite. From current ( $I$ ) – voltage ( $V$ ) characteristics, we observed an ohmic behavior at 300 K for both low and high-current biasing. This behavior turns into nonlinear characteristics when the temperature goes down. As these fabricated structures consist of multiple elementary junctions along the  $c$ -axis, the nonlinear  $I$ - $V$  characteristics result. The impurity assisted interlayer hopping conduction and thermal excitation of carriers play a key role in this effect.

## 5.1. Introduction

Graphite is a well-known three dimensional (3-D) material with a sheet-like layered structure where all the carbon atoms lie in a plane and are weakly bonded to the adjacent graphite sheets [1]. From bulk graphite, graphene (a one atomic thick layer) has recently been cleaved, which emerges as a fascinating material system for fundamental studies in condensed-matter physics [2, 3]. In particular, graphene becomes an active replacement material for silicon which is being used heavily in semiconductor industries nowadays [4]. Each sheet has hexagonal lattice of carbon atoms bonded by strong  $\sigma$  bonding ( $sp^2$ ) in the  $ab$ -plane. The perpendicular  $\pi$ -orbital electrons along the  $c$ -axis are responsible for  $ab$ -plane conductivity [5]. The scientific interest in graphite has recently been renewed by magnetization [6] and transport[7] results on highly oriented pyrolytic graphite (HOPG). Because of the weak interlayer interaction, carrier transport in graphite is essentially two dimensional.

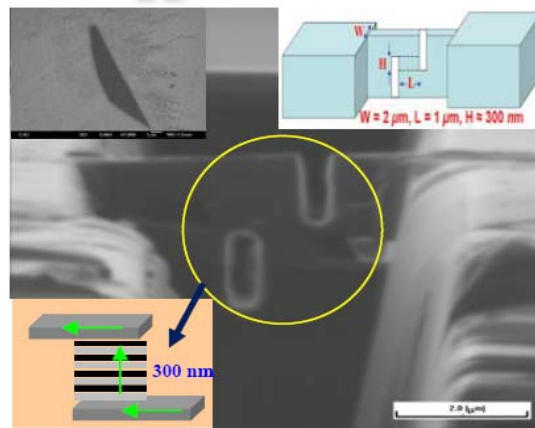
As reported earlier by Primak [8] and Tsang [9] the order of  $c$ -axis resistivity ( $\rho_c$ ) of natural and/or synthetic single crystals of graphite is  $10^{-3} \Omega\text{-cm}$  and shows a metallic temperature ( $T$ ) dependence. But the pyrolytic graphite specimens show  $10\text{-}10^2$  times higher values of  $\rho_c$  than those of single crystals, and exhibit a strange behavior that  $\rho_c$  first increases with increasing  $T$  up to 50 K and then decreases in the following temperature range around it [10, 11]. They show a large electrical anisotropy with a high in-plane conductivity  $\sigma_a \sim 10^4 \Omega^{-1} \text{cm}^{-1}$  and a low  $c$ -axis conductivity  $\sigma_c \sim 10 \Omega^{-1} \text{cm}^{-1}$  at room temperature [12]. Natori et al.[13] reported that the bulk pyrolytic graphite exhibits very large values of anisotropy as  $\rho_c/\rho_a \sim 10^5$  at room temperature and the value of anisotropy of the resistivity decreases with increasing temperature. Graphite shows complicated transport properties concerning magnetic field dependence, conductivity anisotropy and temperature dependence [14].

Although the studies on bulk graphite have been investigated for many years, their transport properties are still not understood well and there has been no work reported yet on the fabrication of planar-type nanostructures along the in-plane and the out-of-plane direction of a thin graphite layer using focused ion beam. In

addition, the temperature- dependent anisotropic transport characteristics for these structures have not been reported elsewhere. Thus, our study is focused on the fabrication of graphite nanostructures using FIB etching technique and their temperature dependent transport characteristics. In this chapter, we report a detailed fabrication and the temperature dependent anisotropic behavior for in-plane and out-of-plane structures fabricated using focused ion beam. We have calculated the resistivity anisotropy ratio  $\rho_c/\rho_a$  for these structures whose values are  $\sim 12.5$  at 300 K and  $\sim 54$  at 25 K. The value of anisotropy increases with decreasing temperature and will be discussed in detail.

## 5.2. Experimental Details

We used mechanical exfoliation technique ( as we mentioned in section 2.3) to extract thin graphite flakes from HOPG, as this method is proven to be a convenient means of selecting single crystallites [15]. We have fabricated several planar-type nanostructures/patterns (along in-plane and out-of-plane) on thin graphite flake using FIB as per procedures followed in the section 2.2. Figure 1 shows the image of out-of-plane (*c*-axis stack) structure.



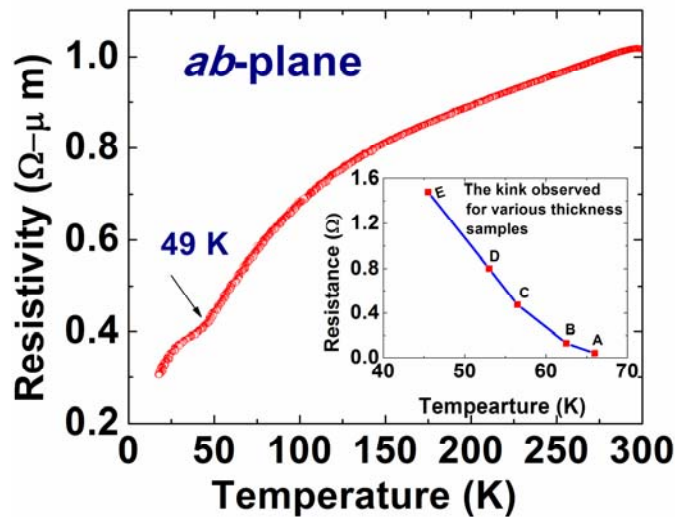
**Figure 1.** The FIB image of fabricated out-of-plane structure (*c*-axis stack). Inset (left bottom) shows the schematic diagram of arrangement of stacked junctions into *c*-axis. The vertical green arrow indicates the current flow direction through *c*-axis stack. Inset (top left) shows the SEM image of thin graphite flake used in this experiment (image scale bar is 1  $\mu\text{m}$ ). The schematic image of fabricated out-of-plane sample geometry and dimensions are given as inset (top right).



The size of the side plane was  $W = 2 \mu\text{m}$ ,  $L = 1 \mu\text{m}$ ,  $H = 300 \text{ nm}$ . The schematic arrangement of stacked junctions is shown in the inset in Figure 1. The FIB fabrication details are reported elsewhere [16]. The electrical transport characteristics were performed for both in-plane and out-of-plane structures by using closed-cycle refrigerator system. Four-probe contacts were made using silver paste and annealed the contacts at  $350 \text{ }^\circ\text{C}$  to avoid the contact resistance.

### 5.3. Results and Discussion

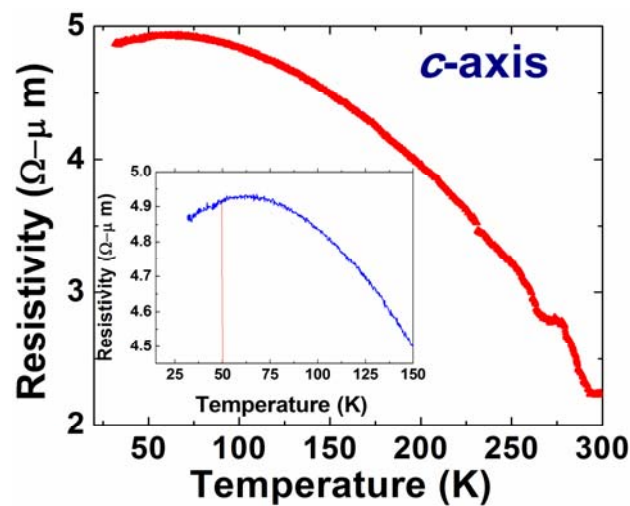
In Figure 2 we show  $R$  vs  $T$  data for the in-plane structure size  $6 \times 2 \mu\text{m}^2$  which exhibits a typical metallic behavior which is similar to the characteristics reported previously for bare graphite flake [17]. We have observed a kink-type structure in the  $R$ - $T$  curves between the temperatures 40 to 70 K for some samples of in-plane fabricated structures. The temperature where the kink-structure appears depends on the sample thickness and resistance. This is plotted in the inset of Figure. 2 for our measured samples A, B, C, D, and E. This small upturn in resistance at low temperature is not yet understood. However, we ensured during measurement that there is no substrate-induced effect behind this kink formation.



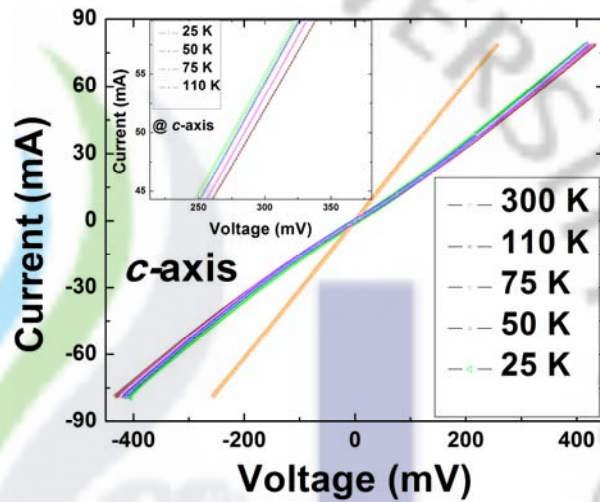
**Figure 2.** The in-plane  $R$ - $T$  characteristics for the structure size  $6 \times 2 \mu\text{m}^2$  which shows typical metallic behavior. Inset plot shows the kink-type structure observed for various samples at different temperatures.

Figure 3 presents the resistance ( $R$ ) – temperature ( $T$ ) characteristics of the out-of-plane structure. With lowering temperature, a semiconducting behavior is observed down to 50 K and then metallic behavior is observed below 50 K. The inset shows the magnified region of  $R$ - $T$  curve which clearly shows the transition at 50 K. This behavior well agrees with earlier observation reported by Matsubara et al.[18] Below 50 K, the impurity-assisted interlayer hopping conduction combined with scattering of carriers can be responsible for the metallic behavior. Above 50 K, thermal excitation of carriers plays a major role for semiconducting temperature dependence [18]. This  $c$ -axis conduction mechanism across the stacking faults aligned  $n$  layers apart, can be explained through the combined effects of tunneling current [19] thermal excitation of carriers over the low potential barrier formed on the plane of stacking disorder [20] and impurity assisted hopping mechanism [21].

The current ( $I$ ) – voltage ( $V$ ) characteristics of the out-of-plane ( $c$ -axis stack) structure is presented in Figure. 4. Most noticeably, we observed linear-ohmic behavior at 300 K for both low and high-current biasing. They turn into nonlinear concave characteristics when the temperature goes down. It is also observed that there is a significant overlap of  $I$ - $V$  curves for temperatures 110 K, 75 K, 50 K and 25 K. It is further noticed that the  $I$ - $V$  curves of these temperatures are appeared with very small difference in  $R$  values. However we observed the higher conductivity at 25 K and 50 K than the conductivity observed at 75 K.

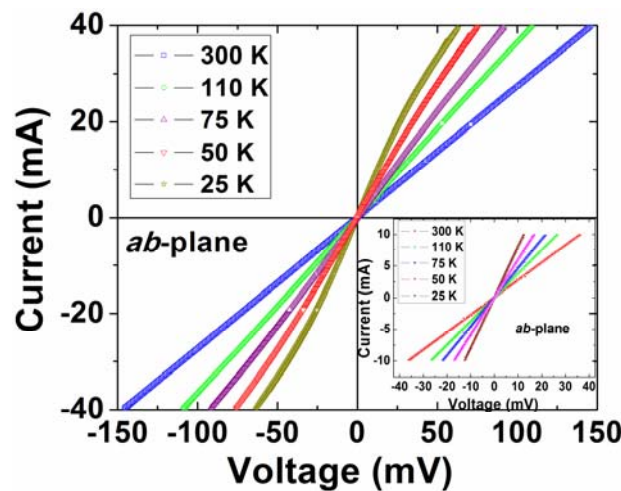


**Figure 3.** The  $R$ - $T$  characteristics for the out-of-plane structure which shows semiconducting behavior till 50 K and then metallic behavior below 50 K. Inset shows a clear transition at 50 K.



**Figure 4.** The  $I$ - $V$  characteristics of out-of-plane ( $c$ -axis stack) structure fabricated on a thin graphite layer. It shows a non-symmetric transition from linear to concave-like nonlinear behavior. Inset show a magnified path of  $I$ - $V$  curves from 25 K to 110 K.

The inset shows a magnified view of  $I$ - $V$  curves indicating the differences in conductance at various temperatures. The voltage shift between them is very small. Since the out-of-plane structure contains multiple elementary junctions along the  $c$ -axis, the nonlinear concave  $I$ - $V$  curves of tunneling characteristics appear. The impurity assisted interlayer hopping conduction and thermal excitation of carriers responsible for  $c$ -axis conduction play a major role in this effect.

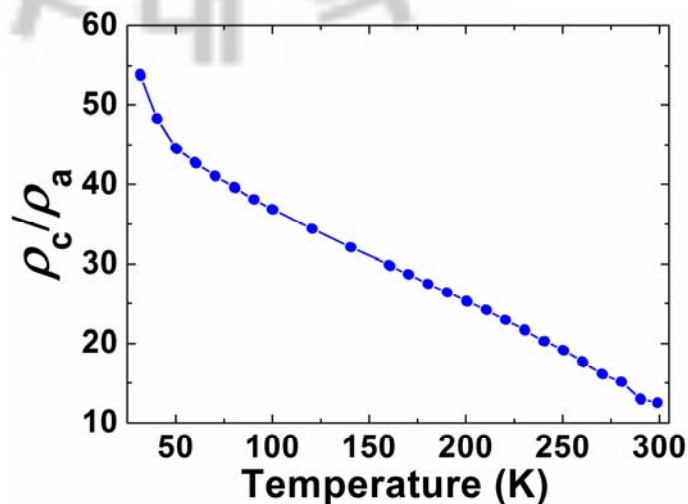


**Figure 5.** The  $I$ - $V$  characteristics of  $6 \times 2 \mu\text{m}^2$  size planar-type structure shows linear-ohmic behavior at 300 K. Inset shows  $I$ - $V$  characteristics of the same sample with low biasing.

In Figure 5 the  $I$ - $V$  characteristics of the  $6 \times 2 \mu\text{m}^2$  size planar-type structure is shown. Similar to out-of-plane, in-plane structures are also shown a linear ohmic behavior at 300 K for both low and high-current biasing which shows a nonlinear convex behavior with decreasing temperature down to 25 K. The low-biasing  $I$ - $V$  characteristics are shown as an inset in Figure 5. No nonlinear behavior is observed when the sample is low-biased. Also, there is no overlap in the  $I$ - $V$  curves for both low and high current biasing. The observed conductivity at 300 K is smaller than the conductivity at lower temperatures. We observed similar characteristics in all other in-plane structures of sizes  $6 \times 6 \mu\text{m}^2$  and  $6 \times 4 \mu\text{m}^2$ .

The appearance of nonlinear  $I$ - $V$  characteristics can be partially possible from the thermal activation as the sample is biased with high-current which could destroy some of parallel conductive paths [22]. As the in-plane and out-of-plane structures show the different convex and concave  $I$ - $V$  characteristics, respectively, it indicates their anisotropic property.

Finally, we have analyzed the temperature dependent resistivity anisotropy data for in-plane and out-of-plane structures which are presented in Figure 6.



**Figure 6.** Plot of the resistivity anisotropy ratio ( $\rho_c/\rho_a$ ) vs temperature for the planar-type nanostructure fabricated on a thin graphite flake.

Both in-plane ( $\rho_a$ ) and out-of-plane ( $\rho_c$ ) resistivities are measured for a sample and the ratio of resistivity anisotropy is determined. The observed in-plane



resistivities are  $17.6 \times 10^{-5} \Omega\text{-cm}$  and  $5.1 \times 10^{-5} \Omega\text{-cm}$  at 300 K and 25 K respectively. Similarly the out-of-plane resistivities are  $213.7 \times 10^{-5} \Omega\text{-cm}$  and  $464.2 \times 10^{-5} \Omega\text{-cm}$  at 300 K and 25 K respectively. The calculated value of anisotropy ratio  $\rho_c/\rho_a$  becomes very small such as  $\sim 12.5$  at 300 K and  $\sim 54$  at 25 K. The observed room temperature anisotropy ratio is varying by a few orders from the values of previously reported anisotropy results of bulk pyrolytic graphite [13]. The decrement of  $\rho_c/\rho_a$  values may be partially arises due to the damage of graphite material as a result of ion beam exposure during fabrication [23]. However, the value of anisotropy increases with decreasing temperature which was an identical behavior to the bulk pyrolytic graphite. The value of resistivity anisotropic ratio for planar-type nanostructures is very smaller than the value of the bulk pyrolytic graphite.

#### 5.4. Conclusion

In summary, we have reported in this chapter the fabrication of planar-type nanostructures (along in-plane and out-of-plane) by using a FIB 3-D etching method and their transport characteristics were discussed. In particular, we observed an ohmic behavior at 300 K for both low and high-current biasing. It turned into nonlinear characteristics when the temperature goes down. Since the fabricated structures have lot of elementary junctions along the  $c$ -axis, the interlayer hopping conduction and thermal excitation of carriers play a key role for this effect. The resistivity anisotropy ratio was determined for these structures. The calculated values of anisotropy ratio  $\rho_c/\rho_a$  were  $\sim 12.5$  at the room temperature and  $\sim 54$  at 25 K. The ratio of resistivity anisotropy increases monotonically with decreasing temperature. The observed value of resistivity anisotropy ratio for the fabricated planar-type nanostructure was few orders smaller than the value of bulk pyrolytic graphite.

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## Chapter 6

### Fabrication and Characteristics of Sub-micron Graphite Stacked-Junctions

In this chapter, we report on the fabrication and transport characteristics of submicron-size stacks along  $c$ -axis of thin graphite flakes. The stacks were fabricated using a three-dimensional focused-ion-beam (FIB) etching technique. The stack with in-plane area  $A$  of  $0.5 \mu\text{m}^2$  showed nonlinear concave-like  $I$ - $V$  characteristics even at 300 K; however the stack with  $A$  of  $> 0.5 \mu\text{m}^2$  were shown an ohmic-like  $I$ - $V$  characteristic at 300 K for both low and high-current biasing. It turned into nonlinear characteristics when the temperature goes down. The in-plane area dependence of stack capacitance were discussed and the observed capacitance of stack with  $A$  of  $0.5 \mu\text{m}^2$  is smaller than the capacitance of stack with  $A$  of  $1 \mu\text{m}^2$  which causes the nonlinear  $I$ - $V$  characteristics in stack with  $A$  of  $0.5 \mu\text{m}^2$  even at 300 K.

## 6.1. Introduction

Graphite is a typical three-dimensional layered-structure semi-metal, consists of stacked layers of multiple graphene sheets held together by weak interlayer interaction force (Van der Waals force) [1]. Each graphite sheet has a hexagonal lattice [2] of carbon atoms bonded by strong  $\sigma$  bonding ( $sp^2$ ) in the  $ab$ -plane. The perpendicular  $\pi$ -orbital electrons along the  $c$ -axis are responsible for the  $ab$ -plane conductance [3]. The research interest in graphite has been renewed by transport results on highly oriented pyrolytic graphite because the carrier transport in graphite is typically two-dimensional [4]. Their electronic transport properties present remarkable scientific and technological potential [5]. While the in-plane transport properties of graphite show an expected metallic character which is reasonably well understood,[6] the carrier transport across the graphitic planes is a contentious issue[7] similar to the issues found in carrier transport in one-dimensional nanostructures[8]. Although many studies have been performed on graphite material, but their transport properties are not yet well understood.

Eventhough the fabrication of graphite-based mesoscopic devices with dimensions of a few tens of nanometers has been reported previously [9], the discovery of novel physical properties has triggered research into few-layer graphite samples and individual graphitic sheets [10]. Many fabrication methods based on high-resolution patterning have been reported to develop high- $T_c$  superconductor devices [11], superconducting-insulating-superconducting (SIS) tunnel junctions using  $e$ -beam lithography [12], submicron tunneling junctions using  $c$ -axis YBCO thin films, Bi-2212 single crystal whiskers [13] and nanopatterns using dual beam focused ion beam [14]. S.-J. Kim *et al* reported that the perfect stacks can be obtained in  $c$ -axis thin films more easily than in  $a$ -axis and single crystal whiskers [15]. However the  $c$ -axis junction fabrication process need to follow hard processes and limits the junction size like mesa structures [16]. Recently the fabrication of graphene-based ultra-capacitors [17] and bi-layer Pseudo-Spin FET (BiSFET) devices [18] were reported elsewhere. FIB micromachining is a direct etching process without use of masking and process chemicals, and demonstrates sub-

micrometer resolution [11]. This technique has also been recognized as a well known fabrication method for making high precision ultra-small devices [19].

The fabrication of a submicron size graphite stacks along *c*-axis using a focused ion beam (FIB) technique has not yet been reported in the literature. Thus in this chapter, we report on the fabrication of submicron size graphite stacks using a focused ion beam (FIB) three-dimensional (3-D) etching method. Also, we present the studies of transport characteristics of submicron stacked-junctions. The in-plane dependence of stack capacitances was also calculated and will be discussed in detail.

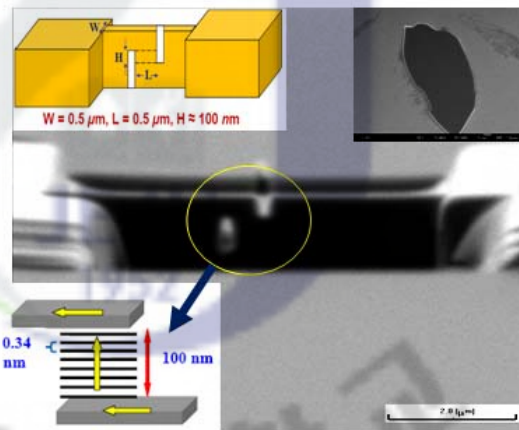
## 6.2. Fabrication of Submicron Stacked-Junctions

We used the mechanical exfoliation technique [10] as mentioned in section 2.3, to obtain micron-scale thin graphite flakes from commercial highly oriented pyrolytic graphite (HOPG) flakes received from *NGS Naturgraphit GmbH*, Germany. The extracted thin graphite crystallites were transferred onto a highly-doped Si substrate with a 300 nm-thick SiO<sub>2</sub> layer. The thicknesses of the graphite flakes were determined to be approximately 500 nm using scanning electron microscope (SEM). Four-probe contacts were made using silver paste and were annealed at 350 °C to avoid contact resistance.

The submicron stack on thin graphite flake was fabricated using a high resolution FIB instrument (SMI-2050 from SII Inc.) as per the procedures followed in the section 2.2. The fabrication parameter for etching process for 30 keV Ga<sup>+</sup> ions was optimized using TRIM simulation [20]. From the simulation results, it was found that for a carbon layer, the low vacancy yield is 92.7 vacancies per ion. Also the maximum penetration depth of 30 keV Ga<sup>+</sup> ions along the *c*- axis of a thin layer is 30 nm and the lateral scattering depth, including the beam spot size, is 20 nm. Therefore the proportion of the fabricated stack affected by ion beam (residual Ga<sup>+</sup>) damage is not so large as well as it does not affect the crystal quality as well.

The lateral dimensions of the sample were  $0.5 \times 0.5 \mu\text{m}^2$ . Figure 1 shows the focused ion microscope view of the fabricated *c*-axis stack on thin graphite flake. The size of the side plane was  $W = 0.5\mu\text{m}$ ,  $L = 0.5\mu\text{m}$ , and  $H = 0.1 \mu\text{m}$ . The *c*-axis length of the stack is approximately  $0.1 \mu\text{m}$ . The schematic arrangement of stacked junctions is shown in the inset (left bottom) in Figure 1. The schematic diagram of

the arrangement of stacked-junctions (with interlayer distance 0.34 nm) in to the  $c$ -axis is shown as inset (left bottom) In Figure.1. The vertical yellow arrow indicates the current flow direction through the submicron stacked-junctions. The schematic image of stack geometry and dimensions are given as inset (top left). The FIB fabrication details are reported elsewhere [21]. The electrical transport characteristics were performed for this stack using closed-cycle refrigerator system (CKW-21, Sumitomo, Japan).



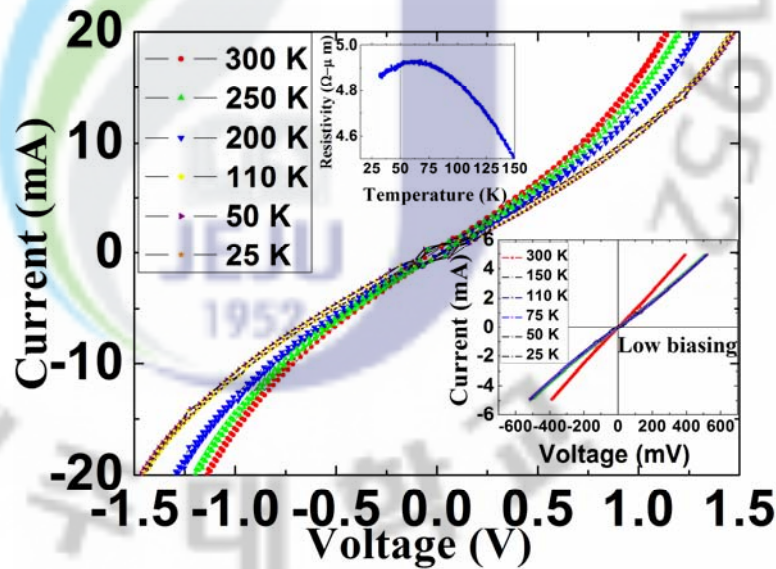
**Figure 1.** The submicron size stack on the thin graphite flake using FIB 3-D etching technique. Inset (top right) shows an SEM image of thin graphite flake used in this experiment (image scale bar is 1  $\mu\text{m}$ ).

### 6.3. Results and Discussion

The current- voltage ( $I$ - $V$ ) characteristics of the fabricated stacks with in-plane area ( $A$ ) of 0.5 and 1  $\mu\text{m}^2$  are presented in Figure 2 and Figure 3 respectively. In Figure 2, the stack (in-plane area of 0.5  $\mu\text{m}^2$ ) showed a nonlinear concave-like  $I$ - $V$  characteristics at all studied temperatures (25 K, 50 K, 110 K, 200 K, 250 K and 300 K) for high biased current (20 mA). For low biased current, it shows linear-ohmic behavior at 300 K and down to 25 K as shown in inset (right bottom) of Figure 2. At 25 K, the stack resistance was found as 75  $\Omega$ . The resistivity versus temperature ( $\rho$ - $T$ ) relation of the submicron stack is shown as inset (top-centre) in Figure.2. We observed a semiconducting behavior till 50 K and then metallic behavior below 50 K.



In the case of stack with  $A$  of  $1 \mu\text{m}^2$  (Figure 3) we observed an ohmic behavior at 300 K for both low and high-current biasing. This leads to nonlinear concave-like characteristics when the temperature goes down. We noticed that there is a significant overlap of  $I$ - $V$  curves for temperatures 110 K, 75 K, 50 K and 25 K. For low-biasing, linear  $I$ - $V$  characteristics are observed at all studied temperatures from 300 K to 25 K which are shown in inset of Figure 3.

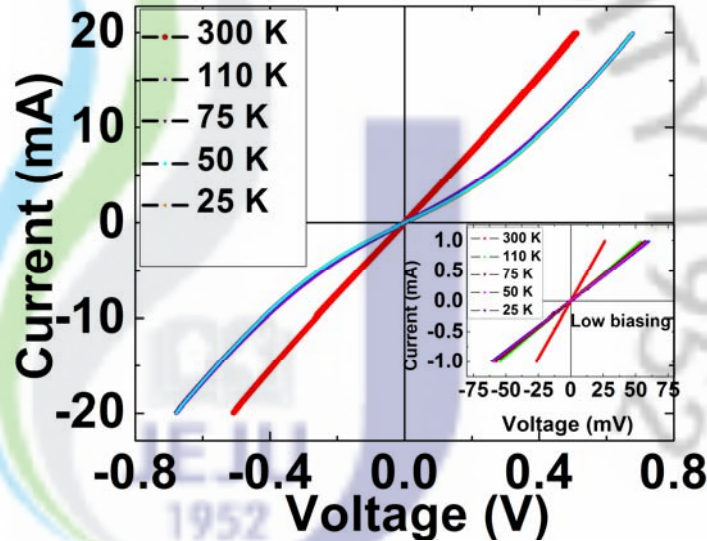


**Figure 2.** The  $I$ - $V$  characteristics of submicron stack with  $A$  of  $0.5 \mu\text{m}^2$  showing nonlinear concave-like characteristics. Inset (top-centre) shows  $\rho$ - $T$  characteristics of submicron-stacked junction.

No nonlinear behavior is observed for the both cases when the sample is low-biased. It is further observed that the  $I$ - $V$  curves of these temperatures have a very small difference in  $R$  values. The voltage shift between them is very small. We observed higher conductivity at 25 K and 50 K than the conductivity observed at 75 K.

Our results of  $c$ -axis stack conduction well agree with earlier observation reported on  $c$ -axis conduction by Matsubara *et al.*[22] Below 50 K, impurity-assisted interlayer hopping conduction combined with scattering of carriers can be responsible for the metallic behavior. Above 50 K, thermal excitation of carriers plays a major role in semiconducting temperature dependence [22]. This  $c$ -axis conduction mechanism across the stacking faults aligned  $n$  layers apart, can be

further explained through the combined effects of tunneling current [23] thermal excitation of carriers over the low potential barrier formed on the plane of stacking



**Figure 3.** The  $I$ - $V$  characteristics of submicron stack with  $A$  of  $1\ \mu\text{m}^2$  shows ohmic behavior at 300 K for both low and high biasing.

disorder [24] and the impurity assisted hopping mechanism [25]. For graphite stacks bigger than  $1\ \mu\text{m}^2$ , we did not observe nonlinear  $I$ - $V$  characteristics at 300 K even at high biasing. With a decrease of the stack size down to  $0.5\ \mu\text{m}^2$ , the junction shows clear nonlinear concave-like  $I$ - $V$  characteristics for both 300 K and 25 K. Since the fabricated stack contains multiple elementary junctions along the  $c$ -axis, the nonlinear concave-like  $I$ - $V$  curves of the tunneling characteristics appear. The appearance of nonlinear  $I$ - $V$  characteristics may be partially due to the thermal activation or self heating effect [26], as the sample is biased with high-current which could destroy some parallel conductive paths [27].

We also explain this behavior in connection with the stack capacitance. Since the stack consists of multiple elementary junctions along the  $c$ -axis, each junction can be considered as a parallel-plate capacitor separated with the interlayer distance of  $0.34\ \text{nm}$ . Assuming the value of dielectric constant  $\zeta_r=1$  (for air between the two layers) and  $\zeta_0 = 8.854 \times 10^{-12}\ \text{F/m}$ , we calculated the capacitance value of these stacks which are presented in Table. I. The capacitance value of stack with  $A$  of  $1\ \mu\text{m}^2$  and  $0.5\ \mu\text{m}^2$  are  $88.5\ \text{aF}$  and  $22.1\ \text{aF}$  respectively. The capacitance of stack with  $A$  of  $0.5$

$\mu\text{m}^2$  is found as smaller than the capacitance value of stack with  $A$  of  $1 \mu\text{m}^2$ . As it is well known, the tunneling current in a tunnel junction of small capacitance  $C$  can be blocked by the charging effect [28] and the charging effects become even stronger in the arrays of the small junctions [29].

**Table I.** Capacitance of different sizes of stacked-junctions

Sample No.	Effective in-plane Area ( $A$ ) ( $\mu\text{m}^2$ )	Stack Height ( $nm$ )	Single junction capacitance ( $C1$ ) ( $fF$ )	Stack capacitance $C = (C1/n)$ ( $aF$ )
1	$1 \times 1$	100	26.4	88.5
2	$0.5 \times 0.5$	100	6.6	22.1

Where  $n$  is the number of junctions in the entire stack.

Thus the whole stack with  $N$  junctions can effectively work as a single unit with the charge energy being  $N$  times higher than the charging energy of a single junction [30]. Due to this reason, the nonlinear characteristics were observed more clearly in the stack with  $A$  of  $0.5 \mu\text{m}^2$  even at 300 K since their capacitance value is very small. With the decrease of  $A$ , the charging energy,  $\Delta V$ , should increase inversely proportional to the stack capacitance,  $C$ , or should be directly proportional to the normal resistance  $R_N$ .

## 6.4. Conclusion

In summary, we demonstrated the fabrication technique for submicron stacked-junctions from thin graphite flake and discussed their transport characteristics by varying the in-plane area down to a submicron scale. The three dimensional FIB fabrication method was discussed in detail in this chapter. The stack with  $A$  of  $0.5 \mu\text{m}^2$  showed nonlinear concave-like  $I-V$  characteristics even at 300 K, however the stacks with  $A$  of  $> 0.5 \mu\text{m}^2$  were shown an Ohmic like  $I-V$  characteristics at 300 K for both low- and high-current biasing. This turned into nonlinear characteristics when the temperature went down. Since the fabricated stacks consist of a lot of elementary junctions along the  $c$ -axis, interlayer hopping conduction and thermal excitation of carriers play a key role in this effect. The in-plane area dependence of stack capacitance were discussed and the observation of

nonlinear characteristics of submicron stacks were explained in connection with the stack capacitance as the capacitance of stack with  $A$  of  $0.5 \mu\text{m}^2$  is found as smaller than the capacitance value of stack with  $A$  of  $1 \mu\text{m}^2$ .

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## Chapter 7

### Investigation of Electrical Transport Characteristics of Nanoscale 3-D Graphite Stacked-Junctions

This chapter presents the fabrication and transport characteristics of nanoscale stacked-junctions of thin graphite flake. The stacked-junctions were fabricated using a three-dimensional focused-ion-beam milling. By varying the effective in-plane area down to submicron scale, the stacked-junctions with in-plane area  $A$  (from 2 down to  $0.25 \mu\text{m}^2$ ) and stack height-length (from 300 to 100 nm) along  $c$ -axis were fabricated. The nano-stack shows perfect  $c$ -axis transport characteristics in which we observed a semiconducting behavior for  $T > 65$  K and metallic behavior for  $T < 65$  K. The obtained results were well fitted with the  $c$ -axis electrical conduction mechanism. The stack with in-plane area  $A$  of  $0.25 \mu\text{m}^2$  showed nonlinear concave-like  $I$ - $V$  characteristics even at 300 K; however the stack with  $A \geq 1 \mu\text{m}^2$  were shown an ohmic-like  $I$ - $V$  characteristic at 300 K for both low and high-current biasing. It turned into nonlinear characteristics when the temperature goes down. The observation of this anomalous transport characteristics were discussed in detail with stack capacitance calculations. The nonlinear characteristics observed at 300 K for the stack with  $A$  of  $0.25 \mu\text{m}^2$  were shown best fit with Fowler-Nordheim tunneling model.

## 7.1. Introduction

Graphite is the oldest well known allotrope of carbon material. In the last 20 years, the discoveries of quasi-zero dimensional buckyballs (fullerenes) [1] and quasi-one dimensional graphene sheets wrapped into cylinders popularly known as carbon nanotubes (CNTs) [2] have resulted in renewed interest in the properties of graphite. Their electronic transport properties present remarkable scientific and technological potential [3-5]. Graphite consists of stacked layers of graphene sheets held together by weak interlayer interaction Van der Waals forces [6]. Each sheet has a hexagonal lattice [7] of carbon bonded by strong  $\sigma$  bonding ( $sp^2$ ) in the in-plane. The perpendicular  $\pi$ -orbital electrons along the  $c$ -axis are responsible for the in-plane conductance. In recent years there have been several studies reported on  $c$ -axis electrical conductivity [8-11], and electric field dependent transport measurements [12]. However the carrier transport across the graphite planes is still a contentious issue [11].

All the previous studies were performed with bulk-sized graphite flakes without following any standard fabrication techniques. As well as, the stack fabrication along  $c$ -axis was not followed by any one of the standard fabrication methods like focused-ion- beam (FIB) or dry etching. However, few reports were available on fabrication of three dimensional (3-D) carbon microstructures using organic precursors [13], and milling of CNTs using FIB [14-16]. Very small structures (in submicron range or below submicron) are needed in the fabrication of tunneling devices and many fabrication methods based on high-resolution patterning have been reported to develop hierarchical and nano-sized pattern formation of nano-track and nano-pore with 100 nm distance using dual beam FIB [17], the fabrication of ultra-thin nano-structured lamellar specimens using FIB scanning electron microscope (SEM) [18] and superconductor-insulator-superconductor tunnel junctions using  $e$ -beam lithography [19]. Using FIB, the perfect stacks can be fabricated in  $c$ -axis thin films more easily than in  $a$ -axis and single crystal whiskers [20]. However the stack fabrication along  $c$ -axis need to follow hard processes and limits the junction size like mesa-structures [21]. FIB micromachining demonstrates sub-micrometer resolution in device fabrication without using process chemicals and mask [22]. Also, this technique has been recognized as a well known fabrication

method for making high precision ultra-small devices [23]. The fabrication of nanoscale stacked-junctions along  $c$ -axis on a thin graphite flake using FIB 3-D milling and their electrical transport studies have not yet been investigated fully.

In this chapter, we present the fabrication of nanoscale graphite stacked-junctions of different effective in-plane area and heights using FIB 3-D milling and their electrical transport characteristics. By varying the effective in-plane area ( $A$ ) down to submicron scale, several stacked-junctions with different stack height (from 300 to 100 nm) were fabricated. A detailed analysis of the electrical transport characteristics of nanoscale stacked-junctions in comparison to the bigger junctions is also presented. The nanostack with  $A \geq 1 \mu\text{m}^2$  shows an ohmic-like characteristics at 300 K for both low and high biasing. However the stack with  $A$  of  $0.25 \mu\text{m}^2$  shows nonlinear characteristics even at 300 K. The observation of this anomalous transport characteristic was discussed in detail with analysis of stack capacitance and proved using Fowler-Nordheim tunneling (FNT) model.

## 7.2. Materials and Methods

In our experiment, we used micromechanical exfoliation method [3, 24] to prepare thin graphite flakes extracted from highly ordered pyrolytic graphite as this method had been known to form perfect crystallites. The extracted thin graphite crystallites were transferred onto a highly-doped Si substrate with a 300 nm-thick thermal oxide layer. Before transferring thin graphite crystallites into substrate, the Si/SiO<sub>2</sub> substrates were cleaned with acetone using an ultrasonic bath for 15 min. The thicknesses of the graphite crystallites were determined to be approximately 500 nm by using SEM. Four probe electrodes (Ag) were fabricated onto the graphite layers. The size of Ag electrode covered on the graphite layer was approximately 25-30  $\mu\text{m}^2$ . We annealed the electrodes at 350 °C for 5 min to avoid the contact resistance. A closed-cycle refrigerator (CCR- SUMITOMO, SRD 204) was used for the low temperature transport measurements. All the measurements were performed between the temperatures 300 K and 25 K. Electrical transport measurements were carried out in Keithley source meters (2400) and nano-voltmeters (2182A). The Raman spectra were recorded with a RENISHAW (M005-141) Raman system with laser frequency

of 514 nm as excitation source. The laser spot size was 1  $\mu\text{m}$  and power at the sample was below 10 mW in order to avoid laser induced heating.

### 7.3. Fabrication of Nano-Stacks

A high resolution FIB instrument (SII NanoTechnology SMI-2050) was used for fabricating graphite nanoscale stacked-junctions. This equipment operates with a 30 keV  $\text{Ga}^+$  ion beam produced by a liquid metal ion source and with maximum probe current of 20 nA. For the smallest beam currents, the beam can be focused down to 5 nm. The etching was optimized for 30 keV  $\text{Ga}^+$  ions using a transport of ions in matter (TRIM) simulation [25]. From this simulation, it was found that for a carbon layer, the low vacancy yield is 92.7 vacancies per ion. Also the maximum penetration depth of 30 keV  $\text{Ga}^+$  ions along the  $c$ -axis is 30 nm and the lateral scattering depth, including the beam spot size, is 20 nm. This standard TRIM simulation results show the proportion of the fabricated stack affected by ion beam (or residual Ga) damage is not so large. (See Figure S1 (a) and (b)).

The ion energy is 30 keV and depth of ion implantation is consistent with 30 nm. We have also run our own TRIM simulations for 30 keV  $\text{Ga}^+$  ions incident at glancing angles. The majority (> 95 %) of  $\text{Ga}^+$  ions are expected to be implanted within 20 nm of the surface, with a much smaller fraction eventually stopping as deep as 30 nm into the surface.

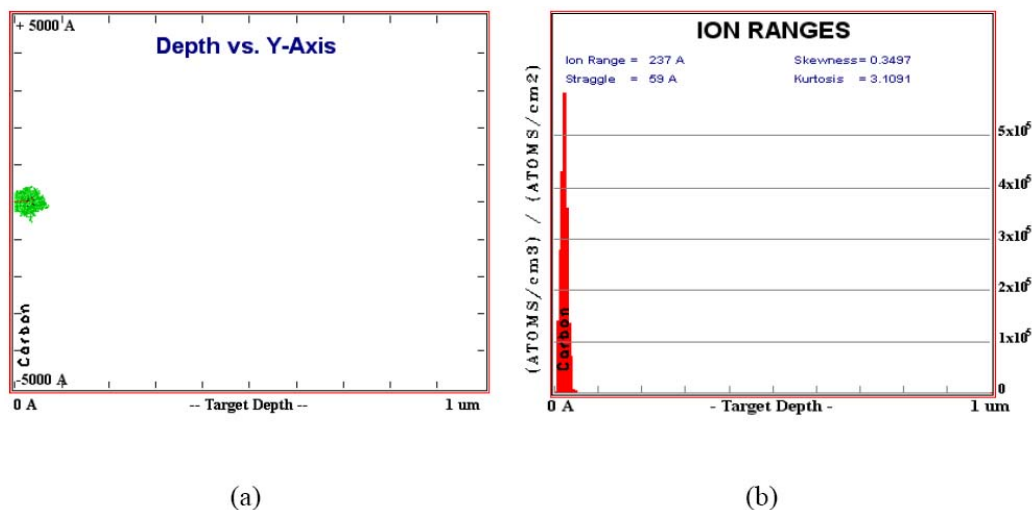


Figure S1

In addition, Raman spectra were taken in order to check the influence of ion beam effect on the graphite surface. It shows *D* band at  $1362\text{ cm}^{-1}$  and other peak at  $2950\text{ cm}^{-1}$  which is due to the  $\text{Ga}^+$  ion implantation during FIB milling. A detailed Raman analysis is given in Figure S4.

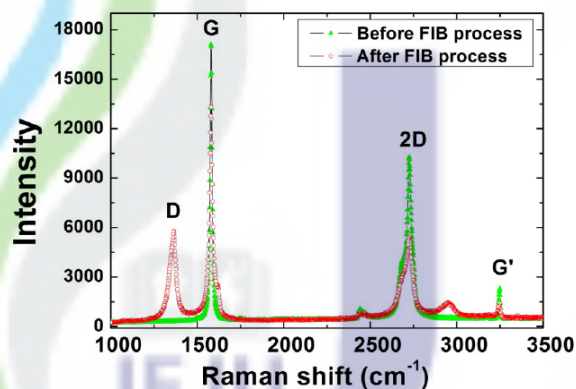


Figure S4

In this case, the Raman spectrum is performed only at the surface of the graphite not at the in-plane area of the junction along the *c*-axis so that the *D* peak arises. Our TRIM simulation results show that the proportion of the fabricated junction affected by ion beam damage is not so large. These results are well agreement with our previously published papers [23, 26].

A graphite flake with the thickness of about 500 nm was chosen for stack fabrication. The stack has an array of graphene sheets with interlayer distance of 0.34 nm. We followed the 3-D milling (as we mentioned in section 2.2) to fabricate the stacked-junctions. We etched the dimensions of  $0.5\ \mu\text{m} \times 0.5\ \mu\text{m}$  along the *ab*-plane direction. The lateral dimensions of the sample were  $0.5 \times 0.5\ \mu\text{m}^2$ . The image of fabricated *ab*-plane structure is shown in Figure 1(a). The SEM image of thin graphite flake is shown as inset in Figure 1(a). The side plane was fabricated and the focused-ion-microscope view of the fabricated *c*-axis stack on thin graphite flake is shown in Figure 1(b).

The fabricated nanoscale stacked-junction (denoted as *J2*) of the dimension of  $W = 0.5\ \mu\text{m}$ ,  $L = 0.5\ \mu\text{m}$ , and  $H = 0.2\ \mu\text{m}$  is shown in Figure 1. The *c*-axis length of the stack is approximately 200 nm. The schematic of the arrangement of stacked-junctions (with interlayer distance 0.34 nm) in to the *c*-axis is shown as inset (top right).



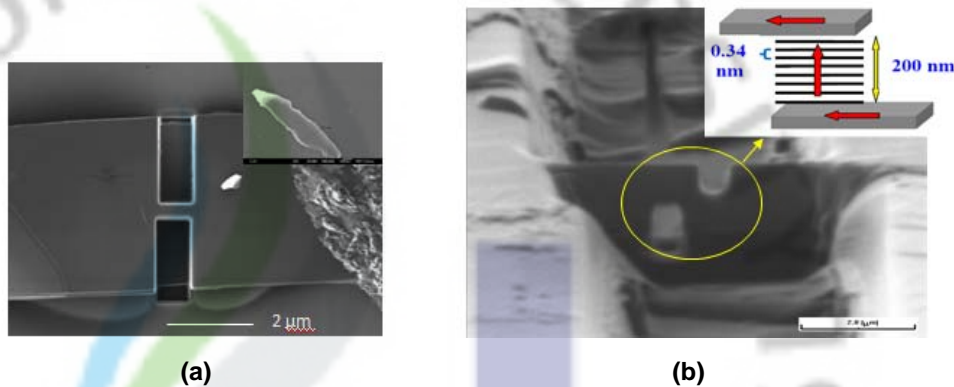


Figure 1. (a) The FIB image of fabricated *ab*-plane structure. In the inset, SEM image of thin graphite flake is shown. (b) The FIB image of fabricated nanoscale stacked-junction (*J2*) with the dimension of  $W = 0.5 \mu\text{m}$ ,  $L = 0.5 \mu\text{m}$ , and  $H = 0.2 \mu\text{m}$ . A schematic for stack arrangement (along *c*-axis) is shown as inset. Current flow direction through the stack is indicated by red arrow.

The vertical red arrow indicates the current flow direction through the nanoscale stack. The detailed FIB fabrication process was discussed elsewhere [26].

Table I. Parameters of nanoscale stacked-junctions with three different nanostacks compared with bigger junctions (*J4* and *J5*).

S. No.	Effective in-plane area (A) ( $\mu\text{m}^2$ )	Stack height (H) (nm)	Resistance of stack ( $R_s$ ) ( $\Omega$ )	Single junction capacitance (C1)(fF)	Stack capacitance $C = (C1/n)$ (aF)	Charging energy $E_c = (e^2/2C)$ (meV)
J1	$0.5 \times 0.5$	100	35.18	6.6	22.619	3.54
J2	$0.5 \times 0.5$	200	75.26	6.6	11.31	7.07
J3	$0.5 \times 0.5$	300	379.9	6.6	7.53	10.06
J4	$1 \times 1$	100	27	26.3	49.4	1.62
J5	$2 \times 1$	300	3.18	52.80	59.79	1.34

By varying in-plane area ( $A$ ) and stack height ( $H$ ), we have fabricated several stacked-junctions with the dimensions of  $W = 0.5 \mu\text{m}$ ,  $L = 0.5 \mu\text{m}$ , and  $H = 0.1 \mu\text{m}$  (denoted as  $J1$ ),  $W = 0.5 \mu\text{m}$ ,  $L = 0.5 \mu\text{m}$ , and  $H = 0.3 \mu\text{m}$  (denoted as  $J3$ ) and two bigger junctions with the dimensions of  $W = 1 \mu\text{m}$ ,  $L = 1 \mu\text{m}$ , and  $H = 0.1 \mu\text{m}$  ( $J4$ ) and  $W = 2 \mu\text{m}$ ,  $L = 1 \mu\text{m}$ , and  $H = 0.3 \mu\text{m}$  ( $J5$ ) as listed in Table. I. The electrical transport characteristics were performed for these stacks and compared their results.

## 7.4. Results and Discussion

### 7.4.1. Current (I) - Voltage (V) characteristics of nanostack

The current-voltage ( $I$ - $V$ ) characteristics of the nanostack with in-plane area ( $A$ ) of  $0.25 \mu\text{m}^2$  ( $J2$ ) at various temperatures, are presented in Figure 2.

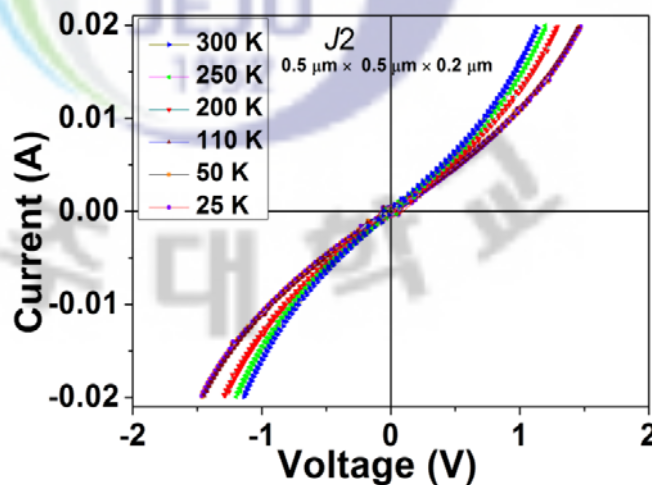


Figure 2.  $I$ - $V$  characteristics of nanostack ( $J2$ ) at different temperature from 25 K to 300 K. The nonlinear characteristics were observed at all studied temperatures.

The stack showed a nonlinear concave-like  $I$ - $V$  characteristics at all studied temperatures (25, 50, 110, 200, 250 and 300 K). At 300 K, the stack resistance was found as  $75 \Omega$ . The stack resistance found increases when the temperature goes down to 25 K. We observed similar nonlinear  $I$ - $V$  characteristics from the nanostacks  $J1$  and  $J3$  at all studied temperatures (from 300 to 25 K).

Next, we compared and analyzed the electrical characteristics of nanostack ( $J2$ ) with bigger junctions  $J4$  ( $1 \times 1 \times 0.1 \mu\text{m}^3$ ) and  $J5$  ( $2 \times 1 \times 0.3 \mu\text{m}^3$ ). We presented the details of junction dimensions and their electrical parameters in Table.

I. From this data, it is clear that the stack with larger height and reduced in-plane effective area ( $A$ ) has shown higher resistance than the stack with larger in-plane area ( $A$ ).

The  $I$ - $V$  characteristics of junctions  $J4$  and  $J5$  at different temperatures are shown in Figure 3 (a) and (b) respectively. We have observed typical  $c$ -axis transport characteristics similar to junction  $J2$ . However the nonlinear  $I$ - $V$  characteristics were not observed at 300 K, but ohmic like-linear behavior is observed. When the temperature goes down, this behavior is turned into curve-like nonlinear characteristics. We noticed that there is a significant overlap of  $I$ - $V$  curves for temperatures 110, 75 and 25 K.

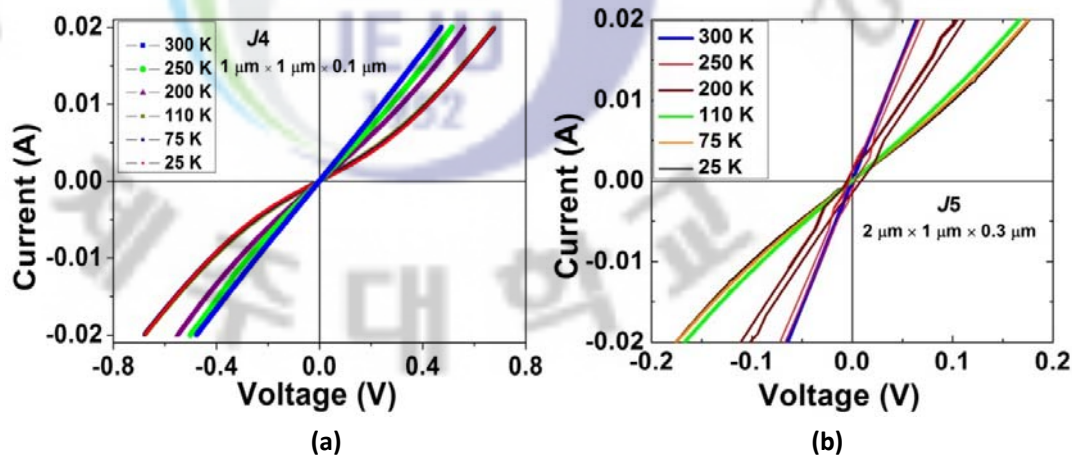


Figure 3. (a)  $I$ - $V$  characteristics of a bigger stacked-junction with  $A$  of  $1 \mu\text{m}^2$  ( $J4$ ) at different temperature from 25 K to 300 K. (b)  $I$ - $V$  characteristics of another bigger junction with  $A$  of  $2 \mu\text{m}^2$  ( $J5$ ) at different temperature from 25 K to 300 K. Both the junctions show ohmic like behavior at 300 K; however the same behavior turned into nonlinear characteristics when the temperature goes down.

It is further observed that the  $I$ - $V$  curves of these temperatures have a very small difference in  $R$  values. The voltage shift between them is very small. This is appeared because of small difference in resistivity values at those temperature region observed from the resistivity versus temperature ( $\rho$ - $T$ ) characteristics. The conduction mechanism across the stacking faults aligned  $n$  layers apart, can be further explained through the combined effects of tunneling current [10], thermal

excitation of carriers over the low potential barrier formed on the plane of stacking disorder [27] and the impurity assisted hopping mechanism [28].

For graphite stacks with  $A \geq 1 \mu\text{m}^2$ , we did not observe nonlinear  $I$ - $V$  characteristics at 300 K even at high biasing (see Figure S2). In Figure S2 the  $I$ - $V$  curve represents the  $I$ - $V$  characteristics of junction  $J5$  at higher bias (maximum current 75 mA is given as input). The bigger junction  $J5$  shows clearly an ohmic-like behavior at 300 K, the same is turned into curve-like nonlinear characteristics when the temperature goes down to 25 K.

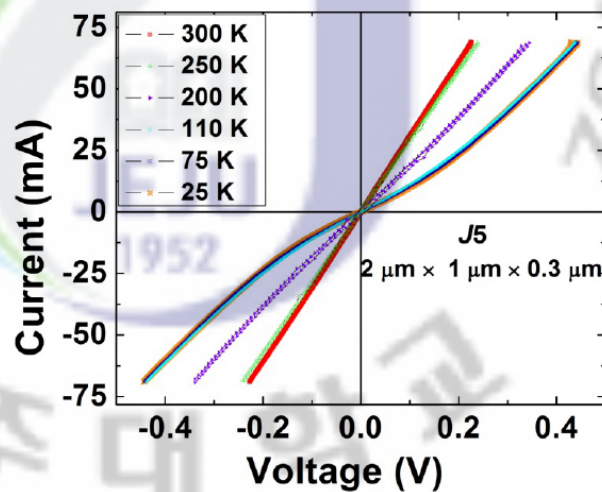


Figure S2

With a decrease of the stack size down to  $0.25 \mu\text{m}^2$ , the junction shows clear nonlinear concave-like  $I$ - $V$  characteristics for both 300 K and 25 K. Since the fabricated stack contains multiple elementary junctions along the  $c$ -axis, the nonlinear concave-like tunneling characteristics appeared from the  $I$ - $V$  characteristics. We discussed the mechanism of nonlinear characteristics and their detailed analysis in later sections 7.4.3 and 7.4.4.

#### 7.4.2. Resistivity ( $\rho$ )-Temperature (T) characteristics of nanostack

Figure 4 represents the  $\rho$ - $T$  characteristics of stacked-junction ( $J2$ ). The junction  $J2$  shows a semiconducting behavior for  $T > 65$  K and metallic characteristics for  $T < 65$  K. Above 65 K, thermal excitation of carriers plays a major role in semiconducting temperature dependence. However below 65 K, the

interlayer hopping conduction combined with scattering of carriers by phonons can be responsible for the metallic-like temperature dependence.

The  $\rho$ - $T$  characteristics along the  $ab$ -plane transport are shown as inset in Figure 4. A well understood metallic behavior is observed. We attempted to fit the  $\rho$ - $T$  data of  $J2$  using the Eqn.1 to explain the electrical conduction mechanism.

$$n \sigma_c = \sigma_{sf} + A \exp(-\Delta E / k_B T) + B \tau_a \quad (1)$$

where  $n \sigma_c$  represents the  $c$ -axis conduction across the stacking faults aligned  $n$  layers apart.  $\tau_a$  is the relaxation time of scattering of carriers in the in-plane conduction.

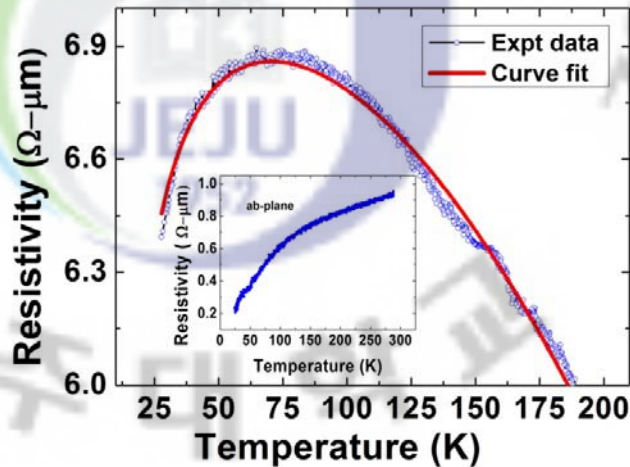


Figure 4. The resistivity ( $\rho$ )-temperature ( $T$ ) characteristics of nanostack ( $J2$ ). A well agreed curve fitting to experimental data is also shown. A clear metallic behavior is observed for  $ab$ -plane transport of bare graphite flake which is shown as inset.

The first term is for the tunneling across the stacking faults which is attributed by tunneling current explained by Ono's theory [10]. The second term is caused by the thermal excitation of carriers over the low potential barrier formed on the plane of stacking disorder [27] and their barrier height ( $\Delta E$ ) is approximately equal to the SW band parameter  $|\Delta| = 0.008$  eV. This represents the potential difference between the two different sites of carbon atoms in the graphite lattice [29]. The temperature dependent coefficient  $A$  is a quantity proportional to the carrier density [30]. When the temperature is above 65 K, the term  $A \exp(-\Delta E / k_B T)$  becomes dominant, thus the value of  $\rho_c$  lowers with increasing temperature in combination with steady increase of the carrier density.



The third term represents the hopping conduction component which is due to the interlayer transfer of charge caused by an interaction between the two-dimensionally delocalized carrier system and any defect and/or impurity sites. The coefficient  $B$  is a quantity proportional to the carrier density which remains constant at low temperature. The relaxation time ( $\tau_a$ ) for the electrical conductivity associated with the scattering of carriers in the in-plane which has the temperature dependence of  $T^{-1}$  [31]. At lower temperature (below 65 K) the localization of charge carriers in the  $c$ -direction takes place. The relaxation time of scattering carriers in the in-plane ( $\tau_a$ ) will be large at lower temperature which results in the decrease in  $c$ -axis resistivity [9]. Thus a metallic behavior was observed below 65 K. This phenomenon is based on the similar conduction mechanism previously observed in graphite intercalated compounds [28, 32].

The stack  $J1$  and  $J3$  have also shown a metal to insulator-like transition similar to  $J2$  and their curve fitted  $\rho$ - $T$  data are given as in Figure S3 (a) and (b). As stack height is increases, the resistance of stack is also increases. The stack with larger height has more number of layers when compared to the stack with lower stack height.

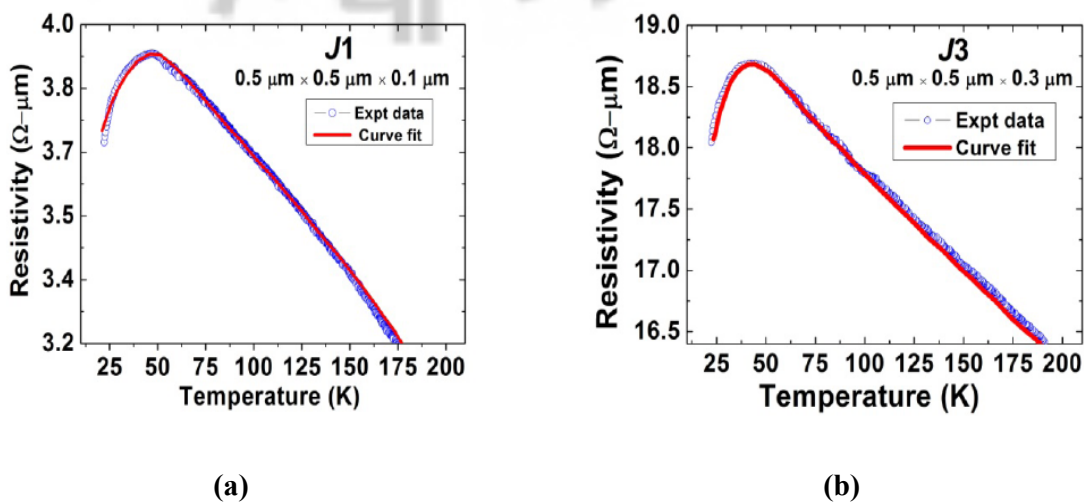


Figure S3

#### 7.4.3. Mechanism behind nonlinear characteristics

The appearance of nonlinear characteristics observed in nanostacks, can be explained in connection with the stack capacitance as well as with FNT model. As the nanostack contains multiple elementary junctions along the  $c$ -axis, each junction

can be considered with two graphite sheets as a parallel-plate capacitor separated with the interlayer distance of 0.34 nm. Hence the entire nanostack can be regarded as an electrical equivalent of capacitors in series (ref. Figure 5(a)) in which each capacitor may work as a tunnel junction. For example, an arrangement of two graphite sheets with an interlayer gap (as insulating region) not only has a resistance, but also a finite capacitance. Increasing the stack height is similar to adding an additional capacitor, which in turn decreasing the stack capacitance and increasing the resistance of stack (ref.  $J1$ ,  $J2$  and  $J3$  data from Table). This is presented in Figure 5 (b).

Assuming the value of dielectric constant  $\zeta_r = 1$  (for air between the two sheets) and  $\zeta_0 = 8.854 \times 10^{-12} \text{ F/m}$ , we calculated the capacitance value of these stacks which are presented in Table. I. The capacitance value of stack with  $A$  of  $2 \mu\text{m}^2$  ( $J5$ ) and  $0.25 \mu\text{m}^2$  ( $J1$ ) are  $59.79 \text{ aF}$  and  $22.1 \text{ aF}$  respectively. The capacitance of stack with  $A$  of  $0.25 \mu\text{m}^2$  ( $J1$ ) is found as smaller than the capacitance value of stack with  $A$  of  $2 \mu\text{m}^2$  ( $J5$ ). If the capacitance is very small, the voltage buildup can be large enough to cause further resistance to charge tunneling.

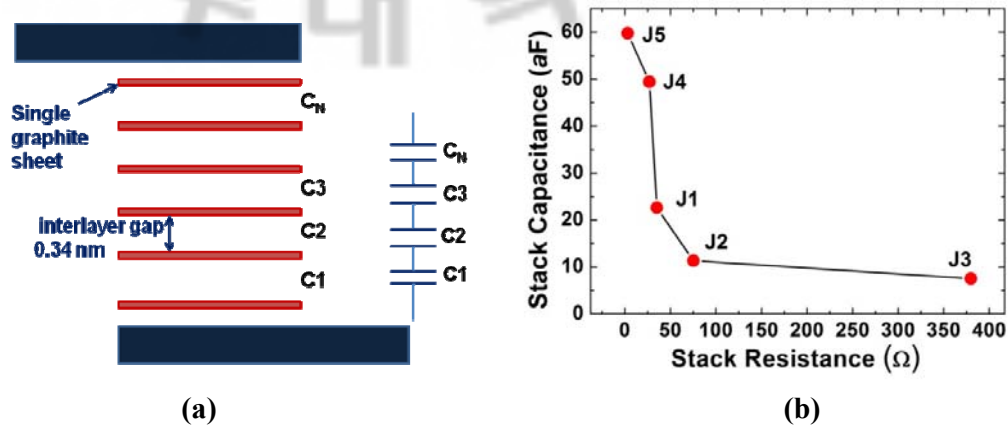


Figure 5. (a) Schematic of stacked-junctions with parallel-plate capacitor arrangement. The nanostack can be regarded as an electrical equivalent of capacitors in series. (b) Plot of stack capacitance versus stack resistance is shown.

As it is well known, the tunneling current in a tunnel junction of small capacitance  $C$  can be blocked by the charging effect [33] and the charging effects become even stronger in the arrays of the small junctions [34] (ref. Table. I). Thus

the whole stack with  $N$  junctions can effectively work as a single unit with the charge energy being  $N$  times higher than the charging energy of a single junction [35]. With the decrease of  $A$ , the charging energy,  $E_c$ , should increase inversely proportional to the stack capacitance,  $C$ , or should be directly proportional to the stack resistance ( $R_s$ ). When a perpendicular electric current is applied through the stack, the potential fluctuations are trapped between the interlayer and its magnitude is increases as the height of stack increases due to their 3-D characters of graphite and existence of parabolic bands [36]. Though the conductivity in  $c$ -axis direction is low enough when compared to in-plane conductivity, it may results electrical resistance between adjacent domains, giving raise to surface potential fluctuations or resistance fluctuations [37, 38]. Hence, the high resistance generated in ultra-small stacked-junctions and their charging energy becomes stronger. Thus the stacks  $J1$ ,  $J2$  and  $J3$  act as high resistive-barriers than stacked-junctions  $J4$  and  $J5$  (see Table. I.). Due to this reason, the nonlinear characteristics were observed more clearly in the stacks with  $A$  of  $0.25 \mu\text{m}^2$  even at 300 K since their capacitance value is very small.

#### 7.4.4. Analysis with Fowler-Nordheim (F-N) Tunneling

FNT model [39] was used to analyze the nonlinear  $I$ - $V$  characteristics observed in nanostacks. In stacked-junctions, the tunneling mechanism can be either direct tunneling or FNT, or a combination of both depending on the magnitude and sign of the applied voltage. In the case of graphite, the tunneling barrier was modelled as triangular in shape [40] with tunnel barrier height  $\Phi$  (work function) of 4.5 eV [41]. Since the tunneling barrier is triangular and  $qV_s \geq \Phi$ , then FNT is said to occur (where  $V_s$  is stack voltage). We presented the F-N plot to experimental  $I$ - $V$  data of stack  $J2$  for various temperatures in Figure 6.

As shown in Figure 6. the F-N plots of  $\ln(I/V^2)$  versus  $I/V$  show good linearity as a sign of FNT mechanism. We find the best fit of the F-N plot to the experimental  $I$ - $V$  data of nanostack  $J2$ . This provides strong evidence for FNT. In case of nanostack  $J1$  and  $J3$  we found the similar fit to their experimental  $I$ - $V$  data. However for the bigger stacked-junction ( $J4$ ), the room temperature  $I$ - $V$  data were not followed F-N plot fitting, which is shown as inset in Figure 6.

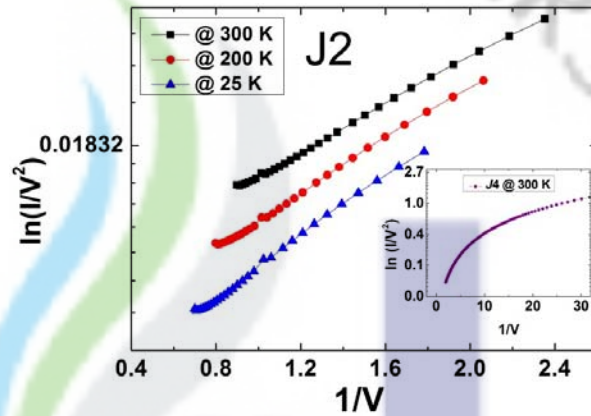


Figure 6. Plot for  $\ln(I/V^2)$  versus  $1/V$  for  $I-V$  data of stack  $J2$  measured at various temperatures. It shows best fit with FNT behavior. Inset shows the F-N plot for junction  $J4$  which does not show F-N fitting for their  $I-V$  data.

Similarly, stack  $J5$  also not shown any fit to F-N plot (data not shown). From the above results, it is clear that the ultra-small stacked-junctions follow the FNT even at 300 K which is one of the evidence for the nonlinear characteristics observed in these stacked-junctions. These observations are evident for experimental analysis of electrical transport characteristics of nanoscale graphite stacked-junctions and suitable for futuristic nonlinear electronic device developments.

## 7.5. Conclusions

In conclusion, we have discussed a precise FIB 3-D milling to fabricate nanoscale stacked-junctions on thin graphite flake. By varying effective in-plane area  $A$  (from 2 down to  $0.25 \mu\text{m}^2$ ) and stack height-length (from 300 to 100 nm), several nano-stacks were fabricated. The electrical conduction mechanism of these stacked-junctions followed a typical  $c$ -axis transport behavior of graphite material. The stack with in-plane area  $A$  of  $0.25 \mu\text{m}^2$  showed clear nonlinear concave-like  $I-V$  characteristics even at 300 K; however the stack with  $A \geq 1 \mu\text{m}^2$  were shown an ohmic-like  $I-V$  characteristic at 300 K. This behavior was further turned into nonlinear characteristics when the temperature goes down. The observation of this anomalous characteristic was explained with in-plane area dependence of stack capacitance and found that stack with in-plane effective area smaller than  $1 \mu\text{m}^2$

showed strong charging effects than the bigger stacks. The observed nonlinearity in  $I$ - $V$  curve of the stack with  $A$  of  $0.25 \mu\text{m}^2$  at 300 K has shown best fit with FNT model. Our results may open road to develop further graphite based nonlinear electronic devices.

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## Chapter 8

### **Electrical Transport Characteristics of Graphene Field Effect Transistors Patterned using Photolithography**

In this chapter, we report on the temperature dependent electrical transport characteristics of graphene field effect transistors (G-FETs) fabricated using photolithographic technique. Monolayer graphene layers were selected for the fabrication of electronic devices and the fabricated devices were further annealed in Ar/H<sub>2</sub> at 200 °C. The temperature dependence of resistance of the graphene flake shows semiconductor-type behavior. The resistance increases about one order of magnitude upon cooling from 300 K to 8 K. Our observations are good in agreement with the previously reported temperature behavior of monolayer graphene nanoribbons and reduced graphene oxide. A higher drain-current modulation in negative back-gate field with current minimum (the Dirac point) is observed at  $V_{GS} \sim -2.75$  V. The carrier mobilities were determined from the measured transconductance and obtained mobilities are less than the conductivity and mobility of pristine graphene. The reason could be discussed in detail with variable range hopping mechanism which is consistent to our resistance/temperature data.

## 8.1. Introduction

Graphene, a single sheet of graphite, receives considerable attention from both physics and technological points of view because of their unique properties arising from its peculiar electronic 2-D band structure, and an extraordinary high carrier mobility of  $200,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  [1]. The unique topology of hexagonal arrangement of carbon atoms provides an unusual energy dispersion relation near the Fermi energy in graphene. The energy dispersion near the charge neutrality points, termed as the Dirac points. [2]. Near the Dirac point, the 2-dimensional (2D) energy spectrum is linear, and thus the electrons always move at the constant speed, the Fermi velocity  $v_F \approx 10^6 \text{ m/sec}$  [3]. In addition, graphene has excellent mechanical and thermal properties [4-5]. It is a semimetal with an extremely small overlap between the valence and the conduction band (zero-gap material). In its 3-D graphite structure, graphene sheets are weakly coupled between the layers with van der Waals forces [6]. The carrier transport in graphene takes place in the  $\pi$ -orbitals perpendicular to the surface [7]. The major advantage of graphene over CNTs is its planar form, which generally allows for highly developed top-down CMOS-compatible process flows. These properties make graphene a promising material for future nano-electronic applications.

There are many approaches reported sofar for graphene synthesis by chemical vapor deposition (CVD) on a substrate [8], sublimating Si from the surface of SiC single crystal [9] and various wet-chemistry based methods [10]. Even the transfer processes used in CVD technique may not be appropriate for applications using a large substrate, including large-scale integrated circuits (LSIs) and large screen displays [11]. We strongly believe that graphene channels should be formed directly on a substrate without such transfer processes. However, up to now no low-cost procedures have delivered high quality graphene for practical electronic device applications. Graphene can be used as the conducting channel for field effect transistors (G-FETs) applications with a variety of gate configuration. Novoselov et al [3] demonstrated the first graphene FET device with back gate configuration on *n*-doped Si substrate and 300 nm thick thermal-oxide SiO<sub>2</sub>. The main advantage of using back gate configuration is the utilization of top surface of graphene for conduction modulation [12]. Lithography-free fabrication techniques have been

reported [13], however the procedures are complicated and yield devices that are restricted to simple geometries [14]. In this presentation, we first describe the sample fabrications processes of single layer graphene devices using lithography followed by metal evaporation and lift off processes. This technique is quite simple, inexpensive when compared to e-beam lithography and CVD techniques. Employing the gate electrode to tune the carrier concentration in graphene, we then discuss temperature dependent transfer characteristics of G-FET from 300 K to 8 K. The carrier mobilities were determined from the measured transconductance. We discuss the conductivity and mobility of graphene devices fabricated through this method. We also describe the effect of fabrication processes on charge carrier mobilities of graphene sample in detail.

## 8.2. Graphene Device Patterning using Photolithography

Highly oriented pyrolytic graphite (HOPG) was used as the source material for graphene fabrication. Graphene flakes were mechanically transferred onto a highly doped silicon wafer according to the method described in [3] as mentioned in the section 2.3. The graphene flakes for device fabrication were chosen by color and contrast according to Refs. [15-16]. We used p-type silicon wafers (100) with a boron doping concentration of  $N_A = 10^{15} \text{ cm}^{-3}$  in which  $\text{SiO}_2$  was thermally oxidized with the thickness of  $t_{\text{ox}} = 300 \text{ nm}$ . The substrate, p +Si (resistivity 1-30  $\Omega \text{ cm}$ ), serves as a back-gate for the FET. To keep the disorder level comparable, we used standard RCA cleaning process followed by acetone and isopropyl alcohol to clean the Si/SiO<sub>2</sub> wafers. Figure 1 represents the optical microscope image of single layer graphene used in this experiment.

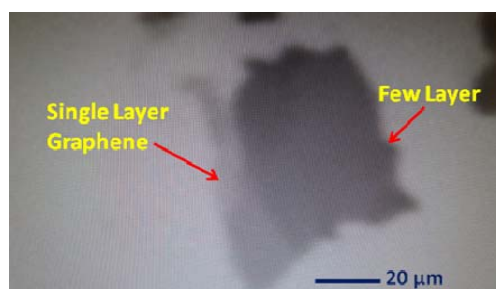


Figure 1. An optical image of single layer graphene is shown. Single and few layer graphene flakes are clearly seen.

We followed the lithographic process described in the section 2.4. The positive photo-resist (AZ 5214) was spin-coated over the graphene flakes on the substrate. By using photolithography (Mask Aligner MDA- 400M; MIDAS), the graphene flakes were patterned through *Cr* mask for electrode formation. Then the gold (99.99 %) electrodes of 100 nm- thick were formed through thermal evaporation technique and structured by lift-off using acetone. A metal contact was made to the substrate as the back-gate contact.

After lift-off process, the device was annealed at 200° C in Ar/H<sub>2</sub> atmosphere for 45 min to improve the adhesion with graphene flake as well as to avoid contaminants [17]. The graphene on the substrates were studied by scanning electron microscopy (SEM: JEOL-6500 field emission scanning electron microscope) and only single layer graphene flakes were selected for this studies. Temperature-dependent transport characterization was carried out using a closed-cycle refrigerator (CKW-21, Sumitomo, Japan) from the temperature 300 K to 8 K. The electrical transport characterization of the back-gated graphene FET devices was carried out using a Keithley instruments (2182 A and 2400 nano-volt and source meters).

### **8.3. Temperature dependent electrical characteristics of graphene**

The typical temperature dependence of resistance of the graphene-FET is presented in Figure 2. The *R-T* characteristics of graphene channel are shown in Figure 2 which exhibits semiconductor-type behavior, so that their resistance increases with decreasing temperature. The resistance increases about one order of magnitude upon cooling from 300 K to 8 K. Our results are in agreement with the previously reported temperature behavior of monolayer graphene nanoribbons produced by chemical unzipping of CNTs [18] and reduced GO [19-20]. As per previous experimental reports, the temperature dependent data for chemically converted graphene could be linearized in  $\ln(I/A)$  versus  $T^{-1/3}$  coordinates, resulting at variable range hopping as a acceptable charge-transport mechanism [20,21].



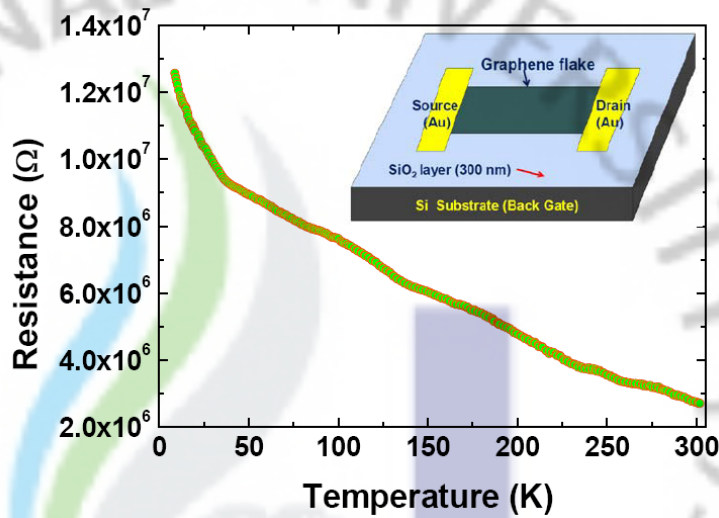


Figure 2. Temperature dependence of resistance of a graphene FET.  $R$ - $T$  characteristics of graphene flake which shows semiconducting behavior. Inset shows schematic picture of the G-FET device used in this experiment.

This obeys temperature dependence:  $I = I_0 \cdot \exp[(T_0/T)^{1/n}]$  where  $(n-1)$  is the dimensionality of the sample [22]. The two-dimensional (2D) character reflected by the observed  $T^{-1/3}$ -dependence is consistent with the 2D structure of our processed graphene. We have also found that our temperature dependent data was linearly fitted in  $\ln(I/A)$  versus  $T^{-1/3}$  coordinates, which is presented in Figure 3.

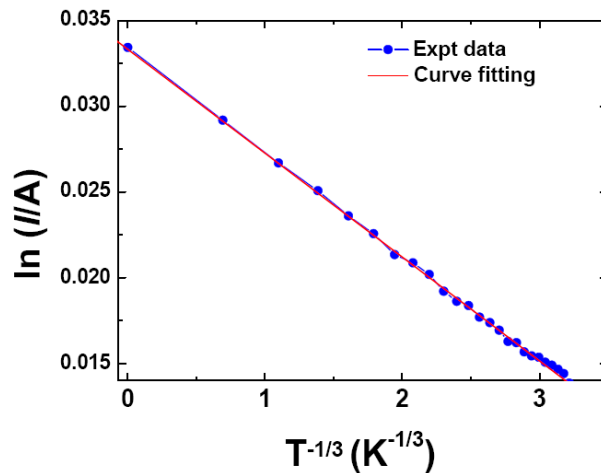


Figure 3. The  $R$ - $T$  data (in figure 2) plotted as a logarithm of current ( $I_{SD}$ ) at  $V_{SD} = 3$  V vs  $T^{-1/3}$ , the solid circles correspond to the experimental data points and the red line is their linear fit.

From this observation, we understand that this variable range hopping mechanism could also be relevant for photo-lithographically fabricated graphene. Our results are well followed the previous observation on chemically converted graphene [18].

The Graphene-FET conductance measurements were performed and the drain-source current was measured with an applied drain-source voltage under different gate voltage tuning. Figure 4 represents the drain-source current ( $I_{DS}$ ) vs the drain-source voltage ( $V_{DS}$ ) under different gate voltages ( $V_{GS} = 0, 6, 10, -6$  and  $-10$  V). The linear  $I_{DS}$  versus  $V_{DS}$  indicates a good ohmic contact between Au contact pads and graphene channel.

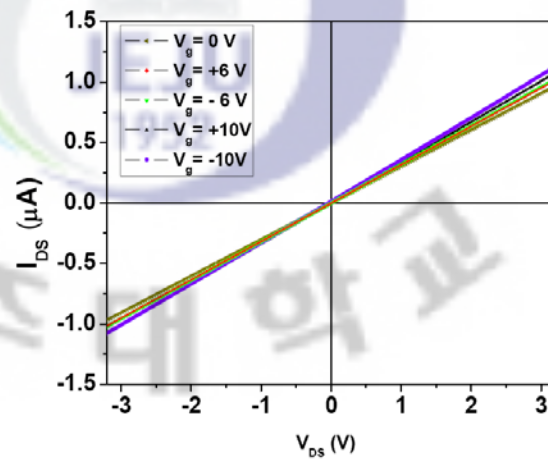


Figure 4. Drain-source current ( $I_{DS}$ ) vs the drain-source voltage ( $V_{DS}$ ) under different gate voltages ( $V_{GS} = 0, 6, 10, -6$  and  $-10$  V) measured at room temperature. A clear linear-ohmic behavior is observed.

#### 8.4. Transfer Characteristics of Graphene FET

Figure 5 represents the room temperature transfer characteristics of source-drain current ( $I_{DS}$ ) dependence on the gate potential ( $V_{GS}$ ) which was recorded at  $V_{DS} = 3$  V. An optical image of graphene patterned with source and drain electrodes having graphene channel width of  $W = 10 \mu\text{m}$ , and the channel length of  $L = 22 \mu\text{m}$  with gate oxide thickness of  $t_{\text{ox}} = 300 \text{ nm}$  is shown in inset of Figure 5.

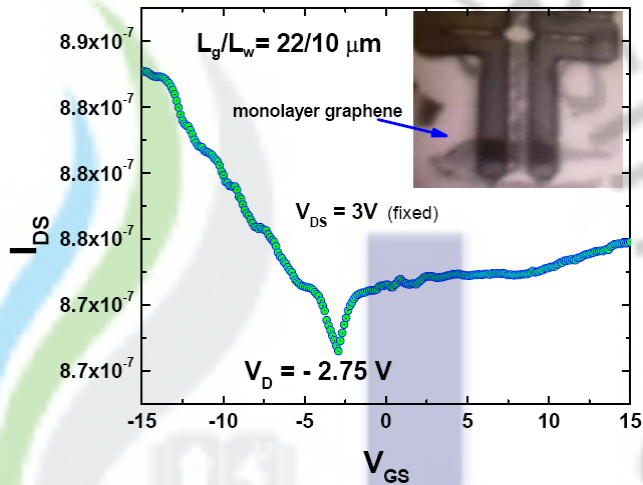


Figure 5. Transfer characteristics of  $I_{DS}$  vs  $V_{GS}$  for a fixed  $V_{DS} = 3$  V,  $V_{GS} = -15$  V to 15 V. The drain-source current  $I_{DS}$  exhibits an ambipolar behavior, both electron and hole conduction, and the current minimum (Dirac point  $V_D$ ) occurs at  $V_{GS} \sim -2.75$  V. Inset shows the graphene with electrode pattern.

The drain-source current was measured with an applied drain-source voltage of 3 V while the gate voltage was swept from -15 V to +15V in order to observe the conductance at neutrality point. An ambipolar electric field behavior is observed which is typical for graphene. While the ambipolar behavior is observed, the hole conduction is favored over the electron conduction. Negative back-gate fields result in higher drain-current modulation compared to positive back-gate fields. For the increasing negative gate fields, a constant increase in hole current is observed. The Dirac point (the current minimum) is observed at the transition point at  $V_{GS} \sim -2.75$  V. The appearance of Dirac point at negative bias region is one of the evidence that the devices have been *n*-doped. The average transconductance per width at  $V_{DS} = 3$  V was extracted to be  $g/W = (dI_{DS}/dV_{GS})/W = 6.5 \mu\text{S/cm}$  for holes and  $4.75 \mu\text{S/cm}$  for electrons.

We have measured the conductivity of G-FET devices and the results suggest that due to high resistance of these monolayer graphene on  $\text{SiO}_2$  (up to 3 M $\Omega$  at room temperature) the contribution from the contacts could be neglected. The room temperature field-effect mobilities extracted from the gate dependences of resistance of monolayer using surface channel device equation 1.

$$\mu = [(\Delta I_d/V_{ds})/(L_w/L_g)]/C_{ox}\Delta V_{gs} \text{ ----- (1)}$$

where  $\mu$  is the carrier mobility,  $L_w$  and  $L_g$  are FET width and gate length respectively.  $C_{ox}$  is determined by  $A\zeta_0\zeta_r/d$  where  $\zeta_0$  is permittivity of free space,  $\zeta_r$  is 3.9 for  $\text{SiO}_2$ ,  $A$  is unit area and  $d$  is gate oxide thickness. The electron and hole mobilities were extracted to be  $\mu_e = 0.303 \text{ cm}^2/\text{V.s.}$  and  $\mu_h = 0.414 \text{ cm}^2/\text{V.s.}$  For most devices the mobilities of holes were slightly higher than those of electrons. The measured values of mobility and conductivity are comparable to the numbers reported for chemically converted graphene produced by GO [20] and monolayer graphene produced by chemical unzipping of CNTs [18]. This result is as expected, considering that single layer graphenes are synthesized with photo-resist and chemical environment during lithographic patterning, the large amounts of oxygen-containing functional groups are attached. Although the annealing of this devices in  $\text{Ar}/\text{H}_2$  environment, the complete removal of these moieties is difficult to achieve [23]. The remaining functional groups may have profound effects on the electronic properties of graphene [24-25]. As graphene consists of a single atomic layer, it is particularly sensitive to surface contaminants, including resist residues left by lithographical processes, which may locally modify the electrochemical potential and provide extra scattering sites [14]. This may contribute to the low values of conductivity and charge carrier mobilities. Suppressed electron conduction in graphene has been predicted theoretically to arise from the chemisorptions of  $\text{H}^+$  on the graphene surface. Our observations are also consistent with the experimental work on organic semiconductors [26] where suppression of electron conduction in organic semiconductors on oxide was attributed to electron trapping by silanol groups. [27].

## 8.5. Conclusion

In summary, we have studied the temperature dependent electrical properties of monolayer graphene-FETs patterned by using photolithographic technique. We observed a semiconducting behavior for their temperature dependent characteristics. These devices on  $\text{Si}/\text{SiO}_2$  substrates exhibit an ambipolar electric field effect (both holes and electron conduction) which are typical for graphene. A clear n-type to p-type transition at Dirac point is observed. The transconductance per width

(6.5  $\mu\text{S}/\text{cm}$ ) and mobility of charge carriers (0.3 to 0.4  $\text{cm}^2/\text{V}\cdot\text{s}$ ) both are much lower than those of pristine graphene. For most devices the mobilities of holes were slightly higher than those of electrons. The measured values of mobility and conductivity are comparable to the numbers reported for chemically converted graphene produced by graphene oxide and monolayer graphene produced by chemical unzipping of CNTs. Since the graphene is particularly sensitive to surface contaminants including resist residues left by lithographical process, which may affect the charge carriers mobility and conductivity and also our temperature/resistance data is consistent with the variable range hopping mechanism. Thus further development of photolithographic techniques to avoid low conductivity and mobility under milder process conditions is in order as this could result in single layer graphene with high mobility and better electronic characteristics.

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## Chapter 9

### Electrical Transport in Graphene-oxide Thin Film Devices

In this chapter, the electrical transport properties of graphene-oxide (GO) thin films were investigated. The GO was synthesized by a modified Hummers method and was characterized by X-ray diffraction and UV-visible spectroscopy. The thin film of GO was made on a Si/SiO<sub>2</sub> substrate by drop-casting. The surface morphology of the GO film was analyzed by using scanning electron microscopy. Temperature dependent resistance and current-voltage measurements were studied using four-terminal method at various temperatures (120, 150, 175, 200, 250 and 300 K) and their charge transport followed the 3D variable range hopping mechanism which was well supported by Raman spectra analysis. The presence of various functional groups in GO were identified by using high resolution X-ray photo electron (XPS) and Fourier transform infra red (FT-IR) spectroscopic techniques. Graphene-oxide thin film field effect transistor devices show p-type semiconducting behavior with a hole mobility of 0.25 cm<sup>2</sup>/V.s and 0.59 cm<sup>2</sup>/V.s when measured in air and vacuum respectively.

## 9.1. Introduction

In recent years, novel carbon-based structures (fullerenes, carbon nanotubes and graphene) represent key materials for new technological device applications. Graphene, a two-dimensional (2D) single atomic layer of  $sp^2$  bonded carbon atoms [1] has been demonstrated as a promising material [2] because of its unique and outstanding electrical [3], thermal [4] and mechanical properties [5]. Its atomic scale thin plane geometry, high carrier mobility and unusual band structure make it an ideal material for applications in future opto-electronic devices [6]. In practice, acquiring large area graphene for future applications such as the integration of high-speed nano-transistors and transparent conducting films are more challenging thing to achieve. One of the alternate methods to prepare graphene nanosheets is achieved by reducing graphene oxide using suitable reducing agents [1, 7]. Graphene oxide (GO) consists of a 2D network of  $sp^2$  and  $sp^3$  bonded atoms, in contrast to an ideal graphene sheet which consists of 100%  $sp^2$  hybridized carbon atoms. The unique atomic and electronic structure of GO [8, 9], consisting of variable  $sp^2 / sp^3$  fractions, opens up possibilities for new functionalities. Most of the  $sp^3$  hybridized carbon atoms are covalently bonded with oxygen in a form of epoxy and hydroxyl groups [10, 11]. GO can be a suitable material with band gap about 1.7 eV at room temperature and acts as a semiconductor [12]. More recently, an attention has turned to GO thin film with intense scientific investigations as it can be used as electron-accepting material in organic solar cells due to its unique structural [13], electronic properties [14], electrochemical active materials [15], cellular imaging and drug delivery applications [16,17].

Recently, few studies were carried out to understand the electrical properties of GO in order to explore the possibility of integrating it with graphene based electronic applications [18,19, 20]. But, the electronic properties and their transport mechanism of GO are not yet explored well. The research on investigation of electrical transport properties of GO thin films has wide potential prospects for futuristic electronic device applications. In this chapter, we report the synthesis and electrical transport mechanism of GO thin films in detail. Temperature dependent transport characteristics (resistance versus temperature (R-T) and current-voltage (I-V) characteristics) were investigated and their transport mechanism was explored using

variable range hopping (VRH) model which was further supported by the Raman spectra analysis.

## **9.2. Experimental Techniques**

### **9.2.1. Materials**

The expandable graphite powder of size lesser than 20  $\mu\text{m}$ , was purchased from Sigma-Aldrich, USA. Sulphuric acid, potassium permanganate and hydrochloric acid were obtained from Daejung Chemicals and Metal Ltd, South Korea. All the chemicals obtained were in research grade. Deionized water was used throughout the experiment.

### **9.2.2. Synthesis of Graphene Oxide**

The GO particles were synthesized by a modified Hummers method [20] as described in section 2.5. The photographic image of uniform GO suspension in water is shown in Figure 1 (a).

### **9.2.3. Characterization Techniques**

X-Ray diffraction characterization was performed on X-ray Diffractometer System, (D/MAX 2200H, Bede 200, Rigagu Instruments C). The UV-Vis spectroscopy was studied using spectrophotometer (Hewlett Packard HP-8453). FT-IR spectroscopy measurement was conducted in FT-IR spectrometer (Model: Bruker IFS 66/S). The surface morphology of GO thin films was analyzed using FE-SEM (JSM-6700F, JEOL Ltd). The GO film thicknesses were measured in reflector-meter (ST4000-DLX; K-MAC Co., Daejeon, Korea) Thin Film Thickness Measurement system [22]. The electrical transport measurements were done in Keithley 2400 source-meter and 2182A nanovolt-meter, which were interfaced with LABVIEW program. A closed-cycle refrigerator (CCR- SUMITOMO, SRD 204) was used for the low temperature transport measurements.

### **9.2.4. Graphene Oxide film formation**

The GO thin film was made by using drop-casting method [23, 24]. The hydrophilicity of GO particles allows it to be adhesive with substrates in the form of

thin film, which is necessary for electronic device applications [9]. Briefly, appropriate amount of GO in 80:20 (v/v) of water and ethanol was sonicated for 30 min for attaining uniform suspension. P-type silicon with 300 nm SiO<sub>2</sub> thermal oxide layer was used as a substrate for GO film deposition. 100 μL of GO dispersion was dropped on to the substrate which was placed on the hot plate and kept at 75 °C. After 20 min, the solvents were evaporated and uniform GO film was formed on the substrate. The thickness of GO film can be controlled by varying the concentration of graphene oxide particles in the dispersion. Four terminal arrangement was used to measure the temperature dependent transport characteristics studies. Silver contacts were made on the GO thin film using thermal evaporation. The device has the dimensions of channel length 800 μm and width 850 μm with thickness of 400 nm. Further GO-FET device was fabricated with source (S) and drain (D) electrodes on Si/SiO<sub>2</sub> substrate with gold back gate (G). The electrodes (source and drain) were made by thermally coated silver of 20 nm thickness. The length and width of the channel of the GO FET device are 60 μm and 50 μm respectively.

### 9.3. Results and Discussion

#### 9.3.1. Characterization of GO Nanoparticles

The XRD pattern of the GO nanoparticles is shown in Fig.1 (b). It shows the diffraction peak at  $2\theta = 10^\circ$  which is mainly due to the oxidation of graphite and the corresponding interlayer spacing was 0.85 nm with the peak (002) [25]. The diffraction peak of pure graphite is found around  $26^\circ$  [26] shown as inset in Fig. 1(b). The disappearance of the peak at  $26^\circ$  and appearance of the peak at  $10^\circ$  show that our product is completely oxidized.

The UV-Vis spectrum of the GO nanoparticles is shown in Fig.1(c). The UV absorption peak is found at 225 nm which is attributed to the  $\pi-\pi^*$  of the aromatic C-C bonds [27]. The presence of oxygenated functional groups in graphene oxide was identified by using FT-IR spectroscopy; the results are shown in Fig. 1 (d). The spectrum shows a broad absorption band at  $3236\text{ cm}^{-1}$ , which is related to the OH groups [28,29,30] and absorption bands at  $1616\text{ cm}^{-1}$ ,  $1730\text{ cm}^{-1}$  and  $1048\text{ cm}^{-1}$  which are typical of carbonyl, carboxyl and C-O-C groups which corresponds well to



reported spectra of GO with oxidized domains [31,32]. Also the complete removal of water content from the GO is practically impossible [33].

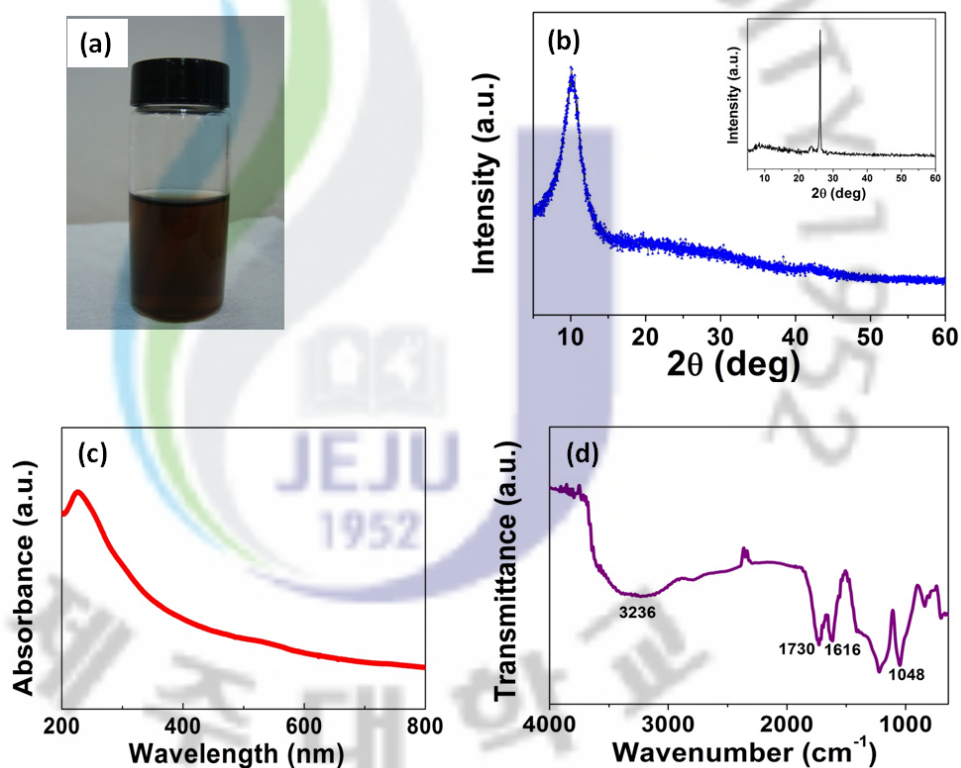


Figure 1. (a) Photographic image of GO dispersion in water (b) XRD of GO nanoparticles. (Inset shows XRD of graphite). (c) UV-Vis spectrum of GO. (d) FT-IR spectrum of GO.

The surface morphology of graphene oxide films is analyzed by using SEM which is shown in Fig. 2. The SEM image exhibits that the prepared graphene oxide film is uniform throughout the surface with little wrinkles on their surface. We prepared GO thin films with the thickness of  $\sim 400$  nm for electrical transport characterization.

### 9.3.2. Temperature Dependent Transport Characterization of GO Thin film

Figure 3 presents the temperature dependent transport characteristics of GO thin film measured using 4-terminal technique. The resistance versus temperature ( $R-T$ ) characteristics of GO thin film is presented in Fig. 3 (a) which exhibits a semiconducting behavior.

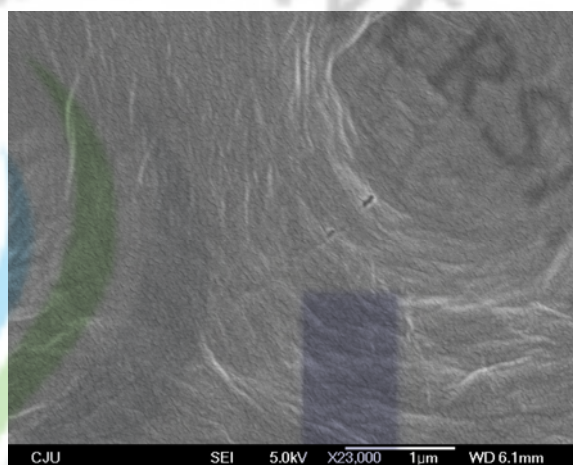


Figure 2. SEM image of GO film deposited on Si/SiO<sub>2</sub> substrate.

While the temperature decreases, the resistance of film increases. The resistance of GO thin film was observed as 10.4 kΩ at 300 K and the same is gradually increased to 1.37 MΩ when the temperature goes down to 120 K. The device resistance increases about three orders of magnitude upon cooling from 300 K to 120 K. The bulk resistivity of the GO thin film was 0.442 Ω-cm at 300 K.

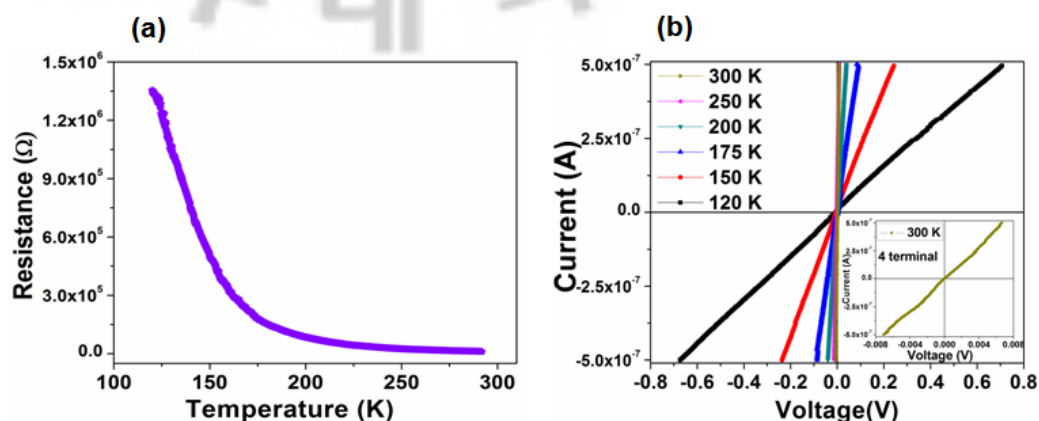


Figure 3. (a) Resistance versus temperature characteristics of GO thin film (b) *I-V* characteristics of the GO thin film measured at various temperatures.

Current versus voltage (*I-V*) characteristics of GO thin film was studied at various temperatures from 300 K to 120 K, which was shown in Fig. 3(b). The magnified graph of *I-V* curve at 300 K is shown in inset in Fig. 3(b). A linear *I-V* behavior was observed at all studied temperatures. These *I-V* graphs confirm the good ohmic

contact between the GO film and electrodes. This results reveal that the nonexistence of Schottky barrier between the electrode contacts and GO thin film.

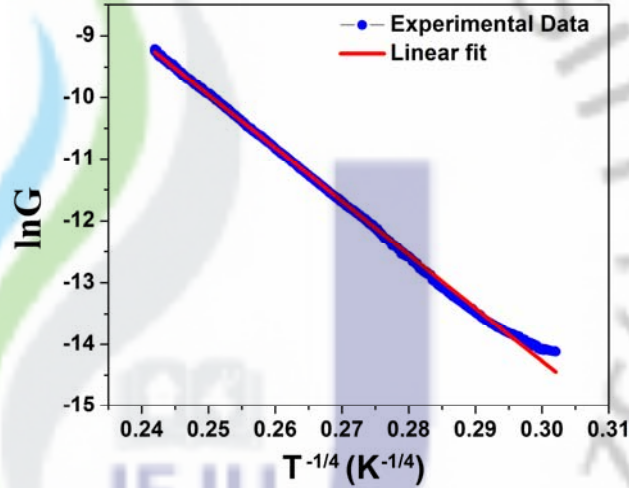


Figure 4. Temperature dependent transport mechanism of GO fitted with VRH model (red line).

The temperature dependent data was fitted to a VRH model to determine the transport mechanism in graphene oxide. Usually VRH involves consecutive inelastic tunneling processes between two localized sites. Hence we investigated our experimental results with VRH model using the general equation [34].

$$I = I_0 \exp \left[ \left( -\frac{T_0}{T} \right)^{1/n} \right] \dots \dots \dots (1)$$

where  $(n-1)$  is the dimensionality of the sample. We have plotted the natural logarithm of the conductance  $\ln G$  as a function of  $T^{-1/4}$  which is shown in Figure 4 along with a best fit line from the VRH model. This is well matched with our experimental results, indicating the charge transport in GO film via many layers with three-dimensional transport behavior.

The VRH conduction mechanism is supported and further confirmed by Raman spectra. The Raman spectra of G, D and 2D bands are shown in Figure 5. The Raman spectra of pristine graphite shows the single crystalline nature of the graphite with in-plane vibrational sharp G band at  $1579 \text{ cm}^{-1}$  and two-phonon 2D band at  $2725 \text{ cm}^{-1}$  which are clearly visible without any indication of disorder D band peak [35,36]. We observed a D band of GO at  $1354 \text{ cm}^{-1}$  [37] as shown in the Figure 5 (a), which is contributed by the functional groups existing in GO. However the 2D

band of GO (Fig. 5(b)) was observed at  $2930\text{ cm}^{-1}$ , which is larger than  $2727\text{ cm}^{-1}$  of pristine graphite, and the observation of peak shift of 2D is tendered by oxygen related functional groups due to the p-doping effect [38,39]. This p-type transport behavior of GO was also observed and presented in later section 9.3.3. This observation confirms the conductance addressed by localized sites existing in the GO film, which is reliable with the VRH conduction mechanism.

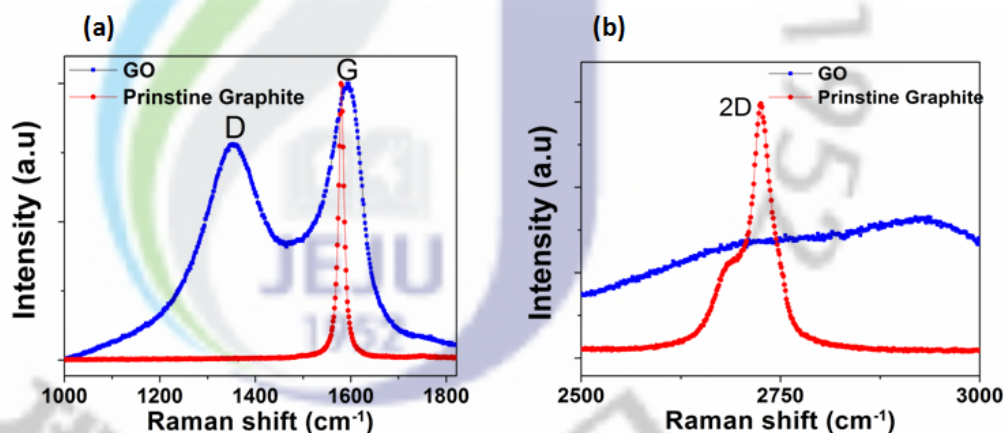


Figure 5. Raman spectra of pristine graphite and GO thin film. (a) Typical D and G spectra (b) 2D spectra of pristine graphite and GO.

To measure the presence of the oxide functional groups, the GO film was characterized by high resolution XPS.

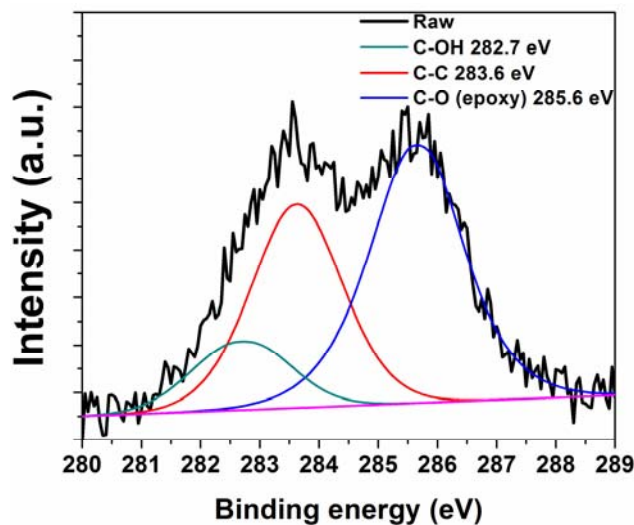


Figure 6. Deconvoluted XPS spectrum of GO

Figure 6 shows the high resolution C 1s XPS spectra of GO film. The GO thin film clearly indicated three main carbon components that correspond to carbon atoms in different functional groups at 282.7, 283.6, and 285.6 eV, corresponding to C–OH, C–C, and C–O groups, respectively. The identification of functional groups using XPS have shown good agreement with the FT-IR spectroscopy results discussed in early part of this chapter.

### 9.3.3. Field Effect Transistor (FET) Characteristics of GO Thin film

In order to find the type of charge carriers and their mobility in graphene oxide, the transfer characteristics of GO FET was investigated. Figure 7 show transfer characteristics of representative GO FETs where current ( $I$ ) is plotted as a function of gate voltage ( $V_G$ ) with fixed source–drain voltage  $V_{DS} = 150$  mV measured in both air and under vacuum. The drain current of GO FET is decreased with the gate voltage as presented in Fig.7, indicating the typical electrical behavior of the p-type FET in which hole carriers play the dominant role in current transport. The p-type semiconducting behavior in graphene oxide FET device is mainly attributed to the polarization of entrapped oxygen groups in between the GO layers. These entrapped oxygen groups which alter the  $sp^2$  hybridized carbon atom in graphite into  $sp^3$  hybridized in graphene oxide during oxidation [40], thereby change the metallic behavior of graphite into a p-type semiconducting behavior. For the measured  $I$ - $V$  characteristics in linear region, the carrier mobilities can be deduced by using equation (3).

$$\mu = \frac{\Delta I_{DS}}{C_{ox} \frac{W}{L} V_{DS} \Delta V_{GS}} \dots\dots\dots(3)$$

where  $\mu$  is the carrier mobility,  $W$  and  $L$  are channel width and length, respectively,  $C_{ox} = \epsilon_{ox} \epsilon_0 / t_{ox}$  is the gate oxide capacitance ( $\epsilon_{ox}=3.9$  is silicon dioxide permittivity and  $t_{ox}$  is the gate oxide thickness), and  $\Delta I_{DS}$  is induced by  $\Delta V_{GS}$ . Using the FET parameters given above, the hole mobilities ( $\mu_h$ ) of the GO device measured in air and vacuum were extracted to be  $0.25 \text{ cm}^2/\text{V.s}$  and  $0.596 \text{ cm}^2/\text{V.s}$  respectively. The GO FET device shows minimum conductance at  $-14.4 \text{ V}$  when measured in air. There are more possibilities for adsorption of molecules like oxygen (which are more electrically sensitive) on the GO surface and the electrodes.



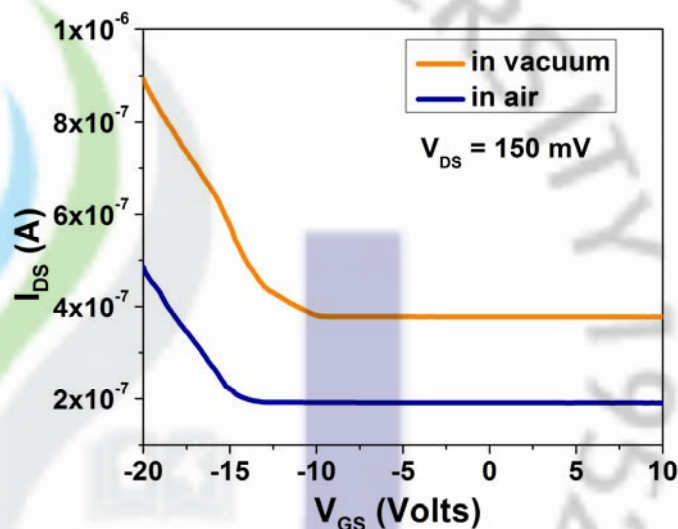


Figure 7. Transfer characteristics ( $I_{DS}$ - $V_{GS}$ ) of GO FET device measured in air and under vacuum at room temperature ( $V_{DS} = 150$  mV).

When the same device is measured in vacuum, the desorption of surface adsorbed molecules takes place, resulting the shift in gate voltage (to  $-10.5$  V) for the minimum conductance. Hence the threshold voltage, defined as the gate voltage  $V_G$ , is shifted from  $-14.4$  V to  $-10.5$  V when the GO FET is measured in vacuum. The increase in mobility of the device and the shift in the point of minimum conductance correspond to the removal of adsorbed species on the surface of the GO. These results are in good agreement with previous studies on graphene oxide based room-temperature gas sensors [41]. Our results on electrical transport characteristics of GO films with the above mentioned advantages ensure the potential applications of GO in future electronic devices.

#### 9.4. Conclusion

In conclusion, we have reported the synthesis and temperature dependent electrical transport properties of graphene oxide thin films. The resistance versus temperature measurement confirmed the semiconducting behavior of GO. The four terminal transport measurements revealed the ohmic linear I-V characteristics at all studied temperatures. Temperature dependent electrical measurements and Raman spectroscopic investigations revealed that the charge transport in GO occurs via

variable range hopping mechanism. The presence of various functional groups in GO was identified by high resolution XPS and FT-IR. The transfer characteristics ( $I_{DS}$ - $V_{GS}$ ) of GO FET device show a more dominating hole conduction over the electron conduction. This  $p$ -type semiconducting behavior of GO arises from the presence of various functional groups in GO. Our investigations on the electrical transport studies of GO films comprising field effect transport properties ensure their potential application in future GO based electronic devices.

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## Chapter 10

### Summary

This chapter summarizes the entire results and over all achievements listed in this thesis. Concluding, this dissertation presented the development of graphitic based devices of the dimensions of stacked-junctions from large in-plane area to nanoscale (submicron and below submicron) with detailed fabrication methods and their electrical transport characteristics results. By varying the stack in-plane area and stack height, the various stacks were fabricated. The stacked-junctions of large in-plane area, submicron-junctions and nanoscale stacked-junctions were fabricated on thin graphite layer.

We have presented a well recognized focused ion beam three-dimensional fabrication technique in detail for fabricating the graphitic stacked-junctions. Detailed electrical transport results of various sizes of these devices were investigated and their results were compared. In this, the transport results of devices for various temperatures from 300 K to 25 K also presented. The temperature dependent transport anisotropy of the graphite planar-type structures was also discussed well.

The preparation and fabrication of the single sheet of graphite, Graphene, was explored very well in this thesis using mechanical exfoliation and photo-lithography techniques followed by metal-evaporation and lift-off processes. The transfer characteristics of graphene field effect transistor devices and their low-temperature transport characteristics of graphene were presented.

Electrical transport in graphene-oxide (GO) thin film devices were presented in detail. In this, the experimental techniques for synthesis of GO, film formation and characterization techniques like XRD, UV-Vis spectrum, FT-IR spectroscopy and SEM. The low-temperature electrical transport characteristics of GO thin films (from 300 K to 120 K) were reported in which the detailed transport mechanism of GO thin film was presented. The resistance (R) -temperature (T) and current (I) and voltage (V) characteristics were discussed in detail. In addition, the GO-field effect transistor characteristics is also studied in this work and reported.



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## **Publications**

### **International Journals**

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2. **Gunasekaran Venugopal**, S.-J. Kim, *Curr. Appl. Phys.* (2011)  
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4. **Gunasekaran Venugopal**, Sang-Jae Kim, *J. Nanosci.Nanotechnol.* 11, 1,

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1. **Gunasekaran Venugopal**, K. Karthikeyan, Rajneesh Mohan, Sang-Jae Kim, “An investigation of electron conduction mechanism of graphene-oxide thin films”

**Domestic Journals**

1. **Gunasekaran Venugopal**, Sang Jae Kim, “Electrical Transport in Submicron stack in thin graphite flake” *Journal of Research Institute of Advanced Technology*, Jeju National University, Vol. 21, 17-22, 2010. ISSN 1598-5849
2. **Gunasekaran Venugopal**, Sang Jae Kim, “Fabrication and Electrical Characteristics of Planar-type graphite nanostructures fabricated by focused ion beam”, *Journal of Research Institute of Advanced Technology*, Jeju National University, Vol. 20, 21-28, 2009. ISSN 1598-5849

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1. **Gunasekaran Venugopal**, Shrikant Saini, Gui-Shik-Kim and Sang-Jae Kim, *The Korea Institute of Applied Superconductivity and Cryogenics* 978-89-957138-2-2, pp 1025-1030 (2009).
2. S. Saini, **Gunasekaran Venugopal**, and S.-J. Kim, *The Korea Institute of Applied Superconductivity and Cryogenics* 978-89-957138-2-2, pp 1007-1011 (2009).
3. **V. Gunasekaran**, S.-J. Kim, "Fabrication of Planar-type Nano Structures on thin Graphite layer using Focused Ion Beam 3-D Etching Technique", *Proceeding of KSPE* (Korean Society for Precision Engineering) Conference Spring 2009, pp. 879-880, Jeju, Korea, June 2009, ISSN 2005-8446. KSPE 09S471, pp.879-880.
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tensile and antibacterial properties”, *Proceeding of KSPE – Spring Conference 2010* (Korean Society for Precision Engineering), Jeju, Korea, May 26-28 2010. pp. 567-568.

11. **Gunasekaran Venugopal**, Sang Jae Kim, "Characterization of graphene oxide transistors” *Proceeding of KSPE – Autumn Conference 2010* (Korean Society for Precision Engineering), Changwon, Korea, Nov. 10-12 2010, KSPE 10A223, pp. 369-370. ISSN 2005-8446.
12. K. Karthikeyan, **Gunasekaran Venugopal**, Sang Jae Kim, "Electrical Characteristics of Graphene oxide” at *KSPE – Autumn Conference 2010* (Korean Society for Precision Engineering), Changwon city, Korea, Nov. 10-12 2010. KSPE 10A222, pp. 367-368. ISSN 2005-8446.
13. **Gunasekaran Venugopal** and Sang-Jae Kim, "Graphene oxide Thin Film Field Effect Transistors”, *Proceeding of 13<sup>th</sup> KMEMS Conference* (Korean MEMS conference) April 2011, KAL Hotel, Jeju, Korea.
14. **Gunasekaran Venugopal**, Sang Jae Kim, "Electrical Transport Characteristics of Graphene oxide Thin films” *Proceeding of KSPE – Spring Conference 2011* (Korean Society for Precision Engineering), Ramada Plaza, Jeju city, Korea, June 1-3, 2011. KSPE 11S619, pp. 615-616. ISSN 2005-8446.

**List of papers presented in Symposia / Conferences/ International Conferences:**

**International Conferences:**

1. Paper presented on “Electrical Transport Measurements of Micrometre Scale Graphite flakes for Micro electronic device applications at “The International Cryogenic Engineering Conference 22 and International Cryogenic Materials Conference (**ICEC22-ICMC 2008**), Seoul, South Korea, (21-25 July 2008).
2. Paper presented on “Characterization of Intrinsic Josephson Junction Stack using High- $T_c$  Superconducting  $\text{Bi}_2\text{Sr}_2\text{CaCu}_2\text{O}_{8+\delta}$ ” at The International Cryogenic Engineering Conference 22 and International Cryogenic Materials Conference (**ICEC22-ICMC 2008**), Seoul, South Korea, (21-25 July 2008)
3. Paper presented on “The observation of diode like characteristics in planar-type Graphite flakes “at The 25<sup>th</sup> International Conference on Low temperature Physics **LT25 – Netherlands**, (6-13 Aug 2008)
4. Paper presented on “ Temperature Dependence of Planar-type Graphite Structures “at The 14th International Symposium on the Physics of



Semiconductors and Applications “ – **ISPSA 2008** conference, Jeju , (26-29 Aug 2008)

5. Paper presented on “Observation of Nonlinear Transport Behavior of Graphite Flakes fabricated by Focused Ion Beam Etching Method” at 7<sup>th</sup> International Conference on New Theories, Discoveries and Applications of Superconductors and Related Materials (**New<sup>3</sup>-SC7**) - Beijing , China ( 13-16, May 2009)
6. Paper presented on “Size dependence of transport characteristics in thin graphite flakes” at International Workshop on Recent Progress in Graphene Research” (**RPGR**) – in Korea Institute for Advanced Study, Seoul, Korea (June 29- July 2, 2009)
7. Paper presented on “Nanoscale fabrication of planar-type patterns on thin graphite flake using focused ion beam 3-D etching technique” at The 7th International Nanotech Symposium & Exhibition in Korea ” (**NANOKOREA-2009**)– in KINTEX, Goyang City, Korea, ( Aug. 26-28, 2009)
8. Paper presented on “Nanoscale fabrication of planar-type structures on thin graphite flake using focused ion beam system” at International Conference on Solid State Devices and Materials (**SSDM**) ” (SSDM -2009)– in Sendai , Japan ( Oct.7-9, 2009)
9. Paper presented on “Fabrication of Nano-stacks on thin graphite layer and observation of size dependent nonlinear transport characteristics” at International Micro processes and Nanotechnology Conference” (**IMNC-2009**) – in Sapporo, Japan (Nov. 16-19, 2009)
10. Paper presented on “Fabrication of Nano-scale Graphite stacks and Observation of anomalous transport behavior” at International Conference on Nano science and Nanotechnology” (**GJ-NST 2009**) – in Muan city, Korea (Nov. 5-6, 2009)
11. Paper presented on “Electrical Transport Characteristics of submicron sized graphite stacks” at The 6<sup>th</sup> International Conference on Advanced Materials and Devices ” (**ICAMD -2009**) – in Jeju city, Korea ( Dec. 9-11, 2009)
12. Paper presented on “Fabrication of Planar-type Graphite Microstructures using Focused Ion Beam 3-D etching technique” at 7th Asian Meeting on Ferroelectricity and 7th Asian Meeting on Electro Ceramics ” (**AMF-AMEC-2010**) – in Ramada plaza, Jeju, Korea ( June 28-July 1, 2010)
13. Paper presented on “Observation of an Anomalous Transport Characteristics of Nanoscale Stacked-Junctions” at 10th Asia-Pacific Conference on Plasma science and technology (APCPST) and 23rd Symposium on Plasma science

for Materials (SPSM) ” (**APCPST-SPSM-2010**) – in Lotte Hotel, Jeju, Korea (July 4-8, 2010). **Selected for Best Poster Award.**

14. Paper presented on "Nanoscale stack fabrication approach towards multi-layer graphene devices using focused ion beam 3-D etching technique", at **IEEE- Nano Korea 2010** conference at Seoul, Korea, Aug. 17-20, 2010.
15. **Oral presentation** on “Nanoscale fabrication of graphite stacked-junctions using Focused Ion Beam and observation of anomalous transport behavior” at 23<sup>rd</sup> international Microprocesses and Nanotechnology Conference (**MNC-2010**), held at Rihga Royal Hotel Kokura, Fukuoka, Japan (Nov. 9-12, 2010).

### **Domestic Conferences:**

1. Technical Paper presented and Participated in “Cavalier Dr. G.K. Devarajulu Technological Excellence Competition 2005” in National Technology Day Celebration, titled on “Phase change optical properties on thin films for rewritable Compact disc applications “at M/s Lakshmi Machine Works Limited, (**LMW**) Coimbatore, India.
2. Paper presented on “ Electronic Transport Properties of Micron Scale Graphite Flakes “ at The **10<sup>th</sup> Korean MEMS (KMEMS)** Conference, Jeju, South Korea., ( 3-4 April 2008).
3. Paper presented on “Quantum Transport Characteristics of Graphene for Nanoelectronic Device Applications “ at The Korean Physical Society – (**KPS-2008**) Physics Conference, Daejeon, South Korea, (17-18 April 2008)
4. Paper presented on “Fabrication of Planar junctions in Graphite sheets using Focused Ion Beam “at The Korean Society of Mechanical Engineers (**KSME-2008**) - Seoul National University, Seoul, South Korea (30<sup>th</sup> May 2008)
5. Paper presented on “Electrical Transport Characteristics of Graphite Planar-type Structures “ in JSST 2008 – The 10<sup>th</sup> Joint Symposium of Jeju National University and Nagasaki University on Science and Technology - at Jeju National University, Jeju , South Korea (4-6 June 2008)
6. Paper presented on “Characterization of planar-type structures in Graphite flakes “ –at The Korean Society for Precision Engineering (**KSPE**) Spring Conference, at Ramada Plaza, Jeju, South Korea (11-13 June 2008).
7. **Oral Presentation** on “Nano scale fabrication and Characterization of graphite planar-type structures “at The 35<sup>th</sup> Annual Conference of the Korean Vacuum Society – (**KVS**) held at Ramada Plaza, Jeju, South Korea (20 – 22 Aug 2008).

8. Paper presented on “Transport Characterization of graphite planar-type micro structures fabricated by Focused Ion Beam “ at The Korean Physical Society – (KPS) Physics Conference , Daejeon, South Korea, (23-24 April 2009).
9. Paper presented on “Fabrication of Planar-type Nano structures on Thin Graphite layer using Focused Ion Beam 3-D Etching Technique “ at Korean Society for Precision Engineering (KSPE) Conference, Ramada Plaza Jeju Hotel, Jeju , South Korea, (3-5 June 2009).
10. Paper presented on “Photolithographic electrode Patterning on graphene and the transport characterization“ at The 11<sup>th</sup> Korean MEMS (KMEMS) Conference, Busan, South Korea., (1-3 April 2010)
11. Paper presented on “Transfer Characteristics of Graphene Field Effect Transistors fabricated using Photolithographic Technique“ at The Korean Physical Society – (KPS-2010) Physics Conference, Daejeon, South Korea, (21-23 April 2010)
12. **Oral presentation** on "Nanoscale Junction Fabrication on Thin Graphite flakes using focused ion beam", at **KSPE** – Spring Conference 2010 (Korean Society for Precision Engineering), Jeju, Korea, May 26-28 2010. pp. 147-148.
13. Paper presented on "Synthesis of MgO/PVA nanocomposite film and investigation on tensile and antibacterial properties", at **KSPE** – Spring Conference 2010 (Korean Society for Precision Engineering), Jeju, Korea, May 26-28 2010. pp. 567-568
14. **Oral presentation** on “Electrical characteristics of in-plane and out-of-plane transport in thin graphite flake” at 2010 Institute of Electrical Engineers, Electronics (Jeju) conference, held at Guest house , Jeju National University, Jeju, South Korea (13 Aug 2010).
15. Paper presented on "Graphene Field effect Transistors”, at **KSME** – Spring Conference 2010 (Korean Society for Mechanical Engineering), ICC, Jeju, Korea, Nov 3-5, 2010.
16. Paper presented on “Graphene oxide Thin Film Field Effect Transistors” at 13<sup>th</sup> **KMEMS** Conference (Korean MEMS conference) April 7-9, 2011, KAL Hotel, Jeju, Korea.
17. Paper presented on “Electrical Transport Characteristics of Graphene oxide thin films “ at Korean Society for Precision Engineering (**KSPE**) Spring Conference 2011, Ramada Plaza Jeju Hotel, Jeju , South Korea, (1-3 June 2011).